RAOUL D. KENNEDY (Bar No. 40892)
DAVID W. HANSEN (Bar No. 196958)
JAMES P. SCHAEFER (Bar No. 250417)
LARA A. ROGERS (Bar No. 261748)
SKADDEN, ARPS, SLATE, MEAGHER & FLOM LLP
Four Embarcadero Center, Suite 3800
San Francisco, California 94111-4144
Telephone: (415) 984-6400
Facsimile: (415) 984-2698
Email: rkennedy@skadden.com; dhansen@skadden.com;
james.schaefer@skadden.com; lrogers@skadden.com

Attorneys for Defendants,
SANDISK CORPORATION and ELIYAHOU HARARI

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

RITZ CAMERA & IMAGE, LLC, a Delaware limited liability company, on behalf of itself and others similarly situated, Plaintiff, v. SANDISK CORPORATION and ELIYAHOU HARARI, Defendants.	CASE NO.: 5:10-CV-02787 JF **REQUEST FOR JUDICIAL NOTICE IN SUPPORT OF DEFENDANTS' MOTION TO DISMISS PLAINTIFF'S FIRST AMENDED COMPLAINT** Date: December 17, 2010 Time: 9:00 AM Judge: Honorable Jeremy Fogel

Pursuant to Rule 201 of the Federal Rules of Evidence, Defendants SanDisk Corporation and Dr. Eliyahou Harari submit this Request for Judicial Notice in support of their Motion to Dismiss Plaintiff's First Amended Complaint ("FAC") and respectfully request that the Court take judicial notice of (1) U.S. Securities and Exchange Commission ("SEC") filings; (2) the three patents identified in the FAC; and (3) the expiration dates of the three patents identified in the FAC.

I. THE COURT SHOULD TAKE JUDICIAL NOTICE OF THE DOCUMENTS SUBMITTED BY DEFENDANTS' IN SUPPORT OF THEIR MOTION TO DISMISS

Judicial notice is proper where a fact is "not subject to reasonable dispute in that it is . . . capable of accurate and ready determination by resort to sources whose accuracy cannot reasonably be questioned." Fed. R. Evid. 201(b). *See Pfannenstiel v. Mortgage Elec. Registration Sys., Inc.*, 2009 WL 347716 (E.D. Cal. Feb. 11, 2009) (granting defendants' request pursuant to Federal Rules of Evidence 201(b), 201(c) and 201(d) to notice public records in support of a motion to dismiss). Further, a court "shall take notice if requested by a party and supplied with the necessary information." Fed. R. Evid. 201(d).

"[R]ecords and reports of administrative bodies" are proper subjects of judicial notice. *Interstate Natural Gas Co. v. S. Ca. Gas Co.*, 209 F.2d 380, 385 (9th Cir. 1953). In particular, "a district court may take judicial notice of the contents of relevant public disclosure documents required to be filed with the SEC as facts capable of accurate and ready determination by resort to sources whose accuracy cannot reasonably be questioned." *In re Silicon Graphics, Inc. Sec. Litig.*, 970 F. Supp. 746, 758 (N.D. Cal. 1997) (citing *Kramer v. Time Warner, Inc.*, 937 F.2d 767, 774 (2d Cir. 1991)); *see also Dreiling v. Am. Exp. Co.*, 458 F.3d 942, 946 n.2 (9th Cir. 2006) (SEC filings subject to judicial notice); *Towantic Energy, L.L.C. v. General Elec. Co.*, 2004 WL 1737254, at *1 n.1 (N.D. Cal. Aug. 2, 2004) (Fogel, J.) (granting Defendant's request for judicial notice of Plaintiff's Form 8-K filed with the SEC).

Likewise, records from the U.S. Patent and Trademark Office ("PTO") are proper subjects of judicial notice. *See Coinstar, Inc. v. Coinbank Automated Systems, Inc.*, 998 F. Supp. 1109, 1114 (N.D. Cal. 1998) (taking judicial notice of U.S. patents).

Accordingly, Defendants request that the Court take judicial notice of the following documents submitted in connection with Defendants' Motion to Dismiss:

1. Exhibit A: Excerpt from SanDisk Corporation's Form 10-K Annual Report Pursuant to Section 13 or 15(d) of the Securities Exchange Act for the fiscal year ended January 3, 2010 (filed with the SEC Feb. 25, 2010);[1]
2. Exhibit B: Excerpt from STMicroelectronics' Form 20-K Annual Report for the fiscal year ended December 31, 2007 (filed with the SEC March 3, 2008);
3. Exhibit C: Excerpt from STMicroelectronics' Form 20-K Annual Report for the fiscal year ended December 31, 2008 (filed with the SEC May 13, 2009);
4. Exhibit D: Excerpt from STMicroelectronics' Form 20-K Annual Report for the fiscal year ended December 31, 2009 (filed with the SEC March 10, 2010);
5. Exhibit E: Excerpt from STMicroelectronics' Form 6-K Report of Foreign Private Issuer Pursuant to Section 13a-16 or 15d-16 of the Securities Exchange Act (dated August 3, 2010);
6. Exhibit F: Excerpt from Micron Technology Inc.'s Form 8-K Current Report Pursuant to Section 13 or 15(d) of the Securities Exchange Act (dated May 7, 2010);
7. Exhibit G: Excerpt from STMicroelectronics' Form 6-K Report of Foreign Private Issuer Pursuant to Section 13a-16 or 15d-16 of the Securities Exchange Act (dated May 4, 2005);
8. Exhibit H: Excerpt from STMicroelectronics' Form 6-K Report of Foreign Private Issuer Pursuant to Section 13a-16 or 15d-16 of the Securities Exchange Act (dated May 19, 2009);
9. Exhibit I: U.S. Patent No. 5,172,338 (the "'338 patent");
10. Exhibit J: U.S. Patent No. 5,991,517 (the "'517 patent");
11. Exhibit K: U.S. Patent No. 5,070,032 (the "'032 patent"); and
12. Exhibit L: PACER Case Locator Civil Case Database Search Results for Party Name "STMicro" and Nature of Suit Code 830 ("Patent") (dated September 30, 2010).

II. THE COURT SHOULD TAKE JUDICIAL NOTICE OF THE EXPIRATION DATES OF THE '338, '517 AND '032 PATENTS

Defendants further request that the Court take judicial notice of the expiration dates of the '338, '517 and '032 patents. Specifically, Defendants request that the Court take notice that the

[1] Due to the voluminous nature of SEC filings and for environmental reasons, Exhibits A through H are limited to the relevant excerpts from STM's SEC filings. Defendants will provide complete copies of these filings if requested by the Court. Complete copies of these SEC filings are also available online at http://www.sec.gov/edgar.shtml.

'338 patent expired December 15, 2009; that the '517 patent expired April 13, 2009; and, that the '032 patent expired March 15, 2009. These dates are appropriate subjects of judicial notice because they are capable of accurate and ready determination by the application of 35 U.S.C. § 154 to the patents. *See Technicon Inst. Corp. v. Alpkem Corp.*, 664 F. Supp. 1558, 1571 (D. Or. 1986) (citing 35 U.S.C. § 154 and taking judicial notice of a patent's expiration date), *aff'd in part, rev'd in part on other grounds, vacated in part*, 837 F.2d 1097 (Fed. Cir. 1987); *Maurice A. Garbell, Inc. v. The Boeing Co.*, 385 F. Supp. 1, 32 (C.D. Cal. 1973) (taking judicial notice of patent's expiration date).

Under 35 U.S.C. § 154(a)(2) the term of a patent resulting from a patent application filed after June 8, 1995 begins on the date of issuance and ends "20 years from the date on which the application for patent was filed in the United States or, if the application contains reference to an earlier filed application or applications . . . from the date on which the earliest such application was filed." 35 U.S.C. § 154(a)(2).

The application resulting in the '517 patent was filed on December 20, 1996, and its term is therefore governed by § 154(a)(2). The '517 patent references U.S. Patent Application No. 07/337,566, filed April 13, 1989, as its earliest parent application. (*See* Ex. K at "Related U.S. Application Data.") Accordingly, under § 154(a)(2), the term of the '517 patent is twenty years from the filing date of the earliest referenced parent application, *i.e.*, twenty years from April 13, 1989. Thus, the '517 patent expired April 13, 2009.

The term of patents either issuing before June 8, 1995 or resulting from applications filed before June 8, 1995, is governed by 35 U.S.C. § 154(c)(1). Under § 154(c)(1), a patent's term "shall be the greater of the 20-year term as provided in subsection (a), or 17 years from grant, subject to any terminal disclaimers." *See also* USPTO, Manual of Patent Examining Procedure § 2701 (explaining calculation of patent term for patents resulting from applications filed before and after June 8, 1995, the date six months after the enactment of the Uruguay Round Agreements Act).

The '338 patent issued December 15, 1992, and its term is, therefore, governed by § 154(c)(1). The earliest patent application referenced in the '338 patent is the 337,579 application

(*See* Ex. J, "U.S. Related Application Data"), which was filed April 13, 1989. Twenty years from that date is April 13, 2009. However, seventeen years from the grant date of the '338 patent is December 15, 2009. Thus, the '338 patent expired December 15, 2009.

The '032 patent's term is also governed by § 154(c)(1) because it issued before June 8, 1995. The application resulting in the '032 patent was filed March 15, 1989, and 20 years from this date is March 15, 2009. The '032 patent does not reference an earlier patent. The '032 patent issued December 3, 1991, and seventeen years from this grant date is December 3, 2008. Thus, because March 15, 2009 is later than December 3, 2008, the '032 patent's expiration date is March 15, 2009.

III. CONCLUSION

For the foregoing reasons, Defendants respectfully requests that the Court take judicial notice of Exhibits A-M attached hereto and of the expiration dates of the '338, '517 and '032 patents.

DATED: October 1, 2010

SKADDEN, ARPS, SLATE, MEAGHER & FLOM, LLP

By: /s/ Raoul D. Kennedy
Raoul D. Kennedy
David W. Hansen

Attorneys for DEFENDANTS,
SANDISK CORPORATION and ELIYAHOU HARARI

EXHIBIT A

UNITED STATES SECURITIES AND EXCHANGE COMMISSION
WASHINGTON, D.C. 20549

FORM 10-K

(Mark One)

☑ **ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

For the fiscal year ended **January 3, 2010**

OR

☐ **TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

For the transition period from to

Commission file number: **0000-26734**

SanDisk®

SANDISK CORPORATION

(Exact name of registrant as specified in its charter)

Delaware	**77-0191793**
(State or other jurisdiction of incorporation or organization)	*(I.R.S. Employer Identification No.)*
601 McCarthy Blvd. Milpitas, California	**95035**
(Address of principal executive offices)	*(Zip Code)*

(408) 801-1000
(Registrant's telephone number, including area code)

Securities registered pursuant to Section 12(b) of the Act:

Title of each class	Name of each exchange on which registered
Common Stock, $0.001 par value; Rights to Purchase Series A Junior Participating Preferred Stock	NASDAQ Global Select Market

Securities registered pursuant to Section 12(g) of the Act: None

Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act. Yes ☑ No ☐

Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Exchange Act. Yes ☐ No ☑

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes ☑ No ☐

Indicate by check mark whether the registrant has submitted electronically and posted on its corporate Website, if any, every Interactive Data File required to be submitted and posted pursuant to Rule 405 of Regulation S-T during the preceding 12 months (or for such shorter period that the registrant was required to submit and post such files). Yes ☐ No ☐

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. ☐

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer, or a smaller reporting company. See definitions of "large accelerated filer," "accelerated filer," and "smaller reporting company" in Rule 12b-2 of the Exchange Act. (Check one):

Large accelerated filer ☑	Accelerated filer ☐	Non accelerated filer ☐	Smaller reporting company ☐
	(Do not check if a smaller reporting company)		

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Exchange Act). Yes ☐ No ☑

As of June 28, 2009, the aggregate market value of the registrant's common stock held by non-affiliates of the registrant was $2,499,682,911 based on the closing sale price as reported on the NASDAQ Global Select Market.

Indicate the number of shares outstanding of each of the issuer's classes of common stock, as of the latest practicable date.

Class	Outstanding at February 1, 2010
Common Stock, $0.001 par value per share	228,717,982 shares

PART I

ITEM 1. *BUSINESS*

Statements in this report, which are not historical facts, are forward-looking statements within the meaning of the federal securities laws. These statements may contain words such as "expects," "anticipates," "intends," "plans," "believes," "seeks," "estimates" or other wording indicating future results or expectations. Forward-looking statements are subject to risks and uncertainties. Our actual results may differ materially from the results discussed in these forward-looking statements. Factors that could cause our actual results to differ materially include, but are not limited to, those discussed in "Risk Factors" in Item 1A, and elsewhere in this report. Our business, financial condition or results of operations could be materially adversely affected by any of these factors. We undertake no obligation to revise or update any forward-looking statements to reflect any event or circumstance that arises after the date of this report. References in this report to "SanDisk®," "we," "our," and "us," collectively refer to SanDisk Corporation, a Delaware corporation, and its subsidiaries. All references to years or annual periods are references to our fiscal years, which consisted of 53 weeks in 2009 and 52 weeks in 2008 and 2007.

Overview

Who We Are. SanDisk Corporation, a global technology company, is the inventor and largest supplier of NAND flash storage card products. Flash storage technology allows digital information to be stored in a durable, compact format that retains the data even after the power has been switched off. Our products are used in a variety of large markets, and we distribute our products globally through retail and original equipment manufacturer, or OEM, channels. Our goal is to provide simple, reliable, and affordable storage solutions for consumer use in a wide variety of formats and devices. We were incorporated in Delaware in June 1988 under the name SunDisk Corporation and changed our name to SanDisk Corporation in August 1995. Since 2006, we have been an S&P 500 company.

What We Do. We design, develop and manufacture data storage solutions in a variety of form factors using our flash memory, proprietary controller and firmware technologies. Our solutions include removable cards, embedded products, universal serial bus, or USB drives, digital media players, wafers and components. Our removable card products are used in a wide range of consumer electronics devices such as mobile phones, digital cameras, gaming devices and laptop computers. Our embedded flash products are used in mobile phones, navigation devices, gaming systems, imaging devices and computing platforms. For computing platforms, we provide high-speed, high-capacity storage solutions known as solid-state drives, or SSDs, that can be used in lieu of hard disk drives in a variety of computing devices.

Most of our products are manufactured by combining NAND flash memory with a controller chip. We purchase the vast majority of our NAND flash memory supply requirements through our significant flash venture relationships with Toshiba Corporation, or Toshiba, which produce and provide us with leading-edge, low-cost memory wafers. From time-to-time, we also purchase flash memory on a foundry basis from NAND flash manufacturers including Toshiba, Samsung Electronics Co., Ltd., or Samsung, and Hynix Semiconductor, Inc., or Hynix. We generally design our controllers in-house and have them manufactured at third-party foundries.

Industry Background

We operate in the flash memory semiconductor industry, which is comprised of NOR and NAND technologies. These technologies are also referred to as non-volatile memory, which retains data even after the power is switched off. NAND flash memory is the current mainstream technology for mass data storage applications and is traditionally used for embedded and removable data storage. NAND flash memory is characterized by fast write speeds and high capacities. The NAND flash memory industry has been characterized by rapid technology transitions which have reduced the cost per bit by increasing the density of the memory chips on the wafer.

Employees

As of January 3, 2010, we had 3,267 full-time employees, including 1,236 in research and development, 443 in sales and marketing, 398 in general and administration, and 1,190 in operations. None of our employees are represented by a collective bargaining agreement and we have never experienced any work stoppage. We believe that our employee relations are satisfactory.

Executive Officers

Our executive officers, who are elected by and serve at the discretion of our board of directors, are as follows (all ages are as of February 15, 2010):

Name	Age	Position
Eli Harari	64	Chairman of the Board and Chief Executive Officer
Sanjay Mehrotra	51	President and Chief Operating Officer
Judy Bruner	51	Executive Vice President, Administration and Chief Financial Officer
Yoram Cedar	57	Executive Vice President, OEM Business and Corporate Engineering

Dr. Eli Harari, the founder of SanDisk, has served as Chief Executive Officer and as a director of SanDisk since June 1988. He was appointed Chairman of the Board in June 2006. Dr. Harari also served as President from June 1988 to June 2006. From 1973 to 1988, Dr. Harari held various technical and management positions with Waferscale Integration, Inc., Honeywell Inc., Intel Corporation and Hughes Microelectronics Ltd. Dr. Harari holds a Ph.D. in Solid State Sciences from Princeton University and has more than 100 patents issued in the field of non-volatile memories and storage systems. Dr. Harari currently serves on the board of directors of Telegent Systems, Inc.

Sanjay Mehrotra co-founded SanDisk in 1988 and has been our President since June 2006. He continues to serve as our Chief Operating Officer, a position he has held since 2001, and he has previously served as our Executive Vice President, Vice President of Engineering, Vice President of Product Development, and Director of Memory Design and Product Engineering. Mr. Mehrotra has 30 years of experience in the non-volatile semiconductor memory industry including engineering and management positions at SanDisk, Integrated Device Technology, Inc., SEEQ Technology, Inc., Intel Corporation and Atmel Corporation. Mr. Mehrotra earned B.S. and M.S. degrees in Electrical Engineering and Computer Sciences from the University of California, Berkeley. He also holds several patents and has published articles in the area of non-volatile memory design and flash memory systems. Mr. Mehrotra currently serves on the board of directors of Cavium Networks and on the Engineering Advisory Board of the University of California, Berkeley.

Judy Bruner has been our Chief Financial Officer and Executive Vice President, Administration since June 2004. She served as a member of our board of directors from July 2002 to July 2004. Ms. Bruner has 30 years of financial management experience, including serving as Senior Vice President and Chief Financial Officer of Palm, Inc., a provider of handheld computing and communications solutions, from September 1999 until June 2004. Prior to Palm, Inc., Ms. Bruner held financial management positions with 3Com Corporation, Ridge Computers and Hewlett-Packard Company. Since January 2009, Ms. Bruner has served on the board of directors and the audit committee of Brocade Communications Systems, Inc. Ms. Bruner holds a B.A. degree in Economics from the University of California, Los Angeles and an M.B.A. degree from Santa Clara University.

Yoram Cedar is our Executive Vice President, OEM Business and Corporate Engineering. Prior to October 2005, Mr. Cedar served as our Senior Vice President of Engineering and Emerging Market Business Development. Mr. Cedar began his career at SanDisk in 1998 when he joined as Vice President of Systems Engineering. He has extensive experience working in product definition, marketing and development of systems and embedded flash-based semiconductors. Prior to SanDisk, he was the Vice President of New Business Development at Waferscale Integration, Inc. and has more than 30 years of experience in design and engineering management of electronic systems. Mr. Cedar earned B.S. and M.S. degrees in Electrical Engineering and Computer Architecture from Technion, Israel Institute of Technology, Haifa, Israel.

EXHIBIT B

As filed with the Securities and Exchange Commission on March 3, 2008

SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

Form 20−F

- **REGISTRATION STATEMENT PURSUANT TO SECTION 12(b) OR (g) OF THE SECURITIES EXCHANGE ACT OF 1934**

OR

- **ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**
  For the fiscal year ended December 31, 2007

OR

- **TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**
  For the transition period from to
- **SHELL COMPANY REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**
  Date of event requiring this shell company report

Commission file number: 1−13546

STMicroelectronics N.V.
(Exact name of registrant as specified in its charter)

Not Applicable	**The Netherlands**
(Translation of registrant's name into English)	*(Jurisdiction of incorporation or organization)*

39, Chemin du Champ des Filles
1228 Plan−Les−Ouates
Geneva
Switzerland
(Address of principal executive offices)

Securities registered or to be registered pursuant to Section 12(b) of the Act:

Title of Each Class:	**Name of Each Exchange on Which Registered:**
Common shares, nominal value €1.04 per share	New York Stock Exchange

Securities registered or to be registered pursuant to Section 12(g) of the Act: None

Securities for which there is a reporting obligation pursuant to Section 15(d) of the Act: None

Indicate the number of outstanding shares of each of the issuer's classes of capital or common stock as of the close of the period covered by the annual report:

899,760,539 common shares at December 31, 2007

Indicate by check mark if the registrant is a well−known seasoned issuer, as defined in Rule 405 of the Securities Act.

Yes • No• •

If this report is an annual or transition report, indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or 15(d) of the Securities Exchange Act of 1934.

Yes • No• •

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days:

Yes • No• •

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non−accelerated filer, or a smaller reporting company. See the definitions of "large accelerated filer," "accelerated filer" and "smaller reporting company" in Rule 12b−2 of the Exchange Act. (Check one):

Large accelerated filer • Accelerated filer • Non−accelerated filer • (Do not check if a smaller reporting company) Smaller reporting company •

Indicate by check mark which financial statement item the registrant has elected to follow:

Item 17 • Item 18• •

PART I

Item 1. Identity of Directors, Senior Management and Advisers

Not applicable.

Item 2. Offer Statistics and Expected Timetable

Not applicable.

Item 3. Key Information

Selected Financial Data

The table below sets forth our selected consolidated financial data for each of the years in the five−year period ended December 31, 2007. Such data have been derived from our Consolidated Financial Statements. Consolidated audited financial statements for each of the years in the three−year periods ended December 31, 2007, including the Notes thereto (collectively, the "Consolidated Financial Statements"), are included elsewhere in this Form 20−F, while data for prior periods have been derived from our Consolidated Financial Statements used in such periods.

The following information should be read in conjunction with "Item 5. Operating and Financial Review and Prospects", the Consolidated Financial Statements and the related Notes thereto included in "Item 8. Financial Information — Financial Statements" in this Form 20−F.

	Year Ended December 31,				
	2007	2006	2005	2004	2003
	(In millions except per share and ratio data)				
Consolidated Statements of Income Data:					
Net sales	$ 9,966	$ 9,838	$ 8,876	$ 8,756	$ 7,234
Other revenues	35	16	6	4	4
Net revenues	10,001	9,854	8,882	8,760	7,238
Cost of sales	(6,465)	(6,331)	(5,845)	(5,532)	(4,672)
Gross profit	3,536	3,523	3,037	3,228	2,566
Operating expenses:					
Selling, general and administrative	(1,099)	(1,067)	(1,026)	(947)	(785)
Research and development(1)	(1,802)	(1,667)	(1,630)	(1,532)	(1,238)
Other income and expenses, net(1)	48	(35)	(9)	10	(4)
Impairment, restructuring charges and other related closure costs	(1,228)	(77)	(128)	(76)	(205)
Total operating expenses	(4,081)	(2,846)	(2,793)	(2,545)	(2,232)
Operating income (loss)	(545)	677	244	683	334
Other−than−temporary impairment charge on financial assets	(46)	—	—	—	—
Interest income (expense), net	83	93	34	(3)	(52)
Earnings (loss) on equity investments	14	(6)	(3)	(4)	(1)
Loss on extinguishment of convertible debt	—	—	—	(4)	(39)
Income (loss) before income taxes and minority interests	(494)	764	275	672	242
Income tax benefit (expense)	23	20	(8)	(68)	14
Income (loss) before minority interests	(471)	784	267	604	256
Minority interests	(6)	(2)	(1)	(3)	(3)
Net income (loss)	$ (477)	$ 782	$ 266	$ 601	$ 253
Earnings (loss) per share (basic)	$ (0.53)	$ 0.87	$ 0.30	$ 0.67	$ 0.29
Earnings (loss) per share (diluted)	$ (0.53)	$ 0.83	$ 0.29	$ 0.65	$ 0.27
Number of shares used in calculating earnings per share (basic)	898.7	896.1	892.8	891.2	888.2
Number of shares used in calculating earnings per share (diluted)	898.7	958.5	935.6	935.1	937.1

development agreement with IBM to develop 32-nm and 22-nm complementary metal-oxide-semiconductor ("CMOS") process technology for 300-mm silicon wafers in order to pursue ongoing core CMOS technology development following the termination of the R&D Crolles 2 Alliance with Freescale Semiconductor and NXP Semiconductors starting this year. We also signed an agreement with IBM to license a derivative technology to implement in our proprietary process for the manufacture of 45-nm integrated circuits. As of December 31, 2007, the residual value, net of amortization, registered in our consolidated balance sheet for these technologies and licenses was $128 million. In addition to amortization expenses, the value of these assets may be subject to impairment with associated charges being made to our Consolidated Financial Statements.

In November 2007 we closed a business acquisition, which included intellectual property and design engineers, in the wireless market for approximately $92 million. In December 2007 we announced, and in January 2008 completed the acquisition of Genesis Microchip Inc. ("Genesis Microchip") for intellectual property related to the digital consumer marketplace and design engineers for $342 million. There is no assurance that such purchases will be successful and will not lead to impairments and associated charges.

The competitive environment of the semiconductor industry may lead to further measures to improve our competitive position and cost structure, which in turn may result in loss of revenues, asset impairments and/or capital losses.

We are continuously considering various measures to improve our competitive position and cost structure in the semiconductor industry.

In 2007 we also made the decision to divest our Flash Memory activities by combining our business with that of Intel and announcing the planned creation of a new independent semiconductor company in the area of Flash memories, which was named Numonyx. The intent is that such new company will benefit from critical size to be competitive in this market. The transaction concerning the creation of Numonyx is planned to close in the first quarter of 2008. There is no assurance that such transaction will close within the timeframe and pursuant to the terms currently planned.

Recently, our sales increased at a slower pace than the semiconductor industry as a whole and our market share declined, even in relation to the markets we serve. Although we recovered in 2006 with an increase in our sales of 11% compared to an increase of 9% for the industry overall, in 2007, our sales increased 1.5% while the industry increased by approximately 3%. There is no assurance that we will be able to maintain or to grow our market share, if we are not able to accelerate product innovation, extend our customer base, realize manufacturing improvements and/or otherwise control our costs. In addition, in recent years the semiconductor industry has continued to increase manufacturing capacity in Asia in order to access lower-cost production and to benefit from higher overall efficiency, which has led to a stronger competitive environment. We may also in the future, if market conditions so require, consider additional measures to improve our cost structure and competitiveness in the semiconductor market, such as increasing our production capacity in Asia, discontinuing certain product families or adding restructurings, which in turn may result in loss of revenues, asset impairments and/or capital losses.

Risks Related to Our Operations

Strategic repositioning may be required, in light of market dynamics, to improve our business performance.

As a result of a strategic review of our product portfolio, we decided in 2007 to divest our Flash Memory activities by combining our business with that of Intel and announcing the planned creation of a new independent semiconductor company in the area of Flash memories, which was named Numonyx. The intent is that such new company will benefit from critical size to be competitive in this market. The transaction concerning the creation of Numonyx is planned to close in the first quarter of 2008. In 2007 we incurred a loss of $1,106 million in connection with this planned transaction. The amount of the loss may increase pending the final evaluation report being prepared by an independent firm, as well as the impact of any further deterioration in the market conditions of the Flash memory business and the credit markets generally. Further, if the transaction is postponed or not consummated as planned, we may incur additional charges. Once Numonyx begins operations, we may also incur losses proportionate to our equity holding in this company.

Additionally, we are constantly monitoring our product portfolio and cannot exclude that additional steps in this repositioning process may be required; further, we cannot assure that the strategic repositioning of our business will be successful and produce the planned operational and strategic benefits and may not result in further impairment and associated charges.

seek to enhance our competitive position on all fronts of the memory market we serve both by adding new products and improving manufacturing costs.

We expect to deconsolidate this group with the closing of the Numonyx transaction planned for the first quarter of 2008. From that point forward, our Flash memory exposure will consist of our 48.6% equity interest in Numonyx and will be reported in the Earnings/Loss on equity investments line item on our consolidated statement of Income, and certain financing arrangements.

Strategic Alliances with Customers and Industry Partnerships

We believe that strategic alliances with customers and industry partnerships are critical to success in the semiconductor industry. We have entered into several strategic customer alliances, including alliances with Alcatel-Lucent, Bosch, Hewlett-Packard, Marelli, Nokia, Nortel, Pioneer, Seagate, Continental AG, Thomson and Western Digital. Customer alliances provide us with valuable systems and application know-how and access to markets for key products, while allowing our customers to share some of the risks of product development with us and to gain access to our process technologies and manufacturing infrastructure. We are actively working to expand the number of our customer alliances, targeting OEMs in the United States, in Europe and in Asia and our recently announced digital base-band relationship with Ericsson Mobile Platform is an example of our success in formalizing this program.

Partnerships with other semiconductor industry manufacturers permit costly research and development and manufacturing resources to be shared to mutual advantage for joint technology development. We have a long history of partnership for the collaborative development of CMOS process technologies in Crolles, France. Since January 1, 2008, we are collaborating with IBM on the development of 32-nm and 22-nm CMOS process technologies. We will pursue the development, with IBM, of CMOS derivatives in Crolles. This cooperation follows the termination at the end of 2007 of the cooperation with Freescale Semiconductor and NXP Semiconductors for the joint research and development of advanced CMOS process technology on 300-mm wafers, as well as for the operations of a 300-mm wafer pilot line fab which has been built in Crolles2. We remain convinced that the shared R&D business model contributes to the fast acceleration of semiconductor process technology development and we will continue to actively pursue an expansion of our portfolio of alliances to reinforce cooperation in the area of technology development in Crolles2.

We have also established joint development programs with leading suppliers such as Air Liquide, Applied Materials, ASM Lithography, Canon, Hewlett-Packard, KLA-Tencor, LAM Research, MEMC, Teradyne and Siltronics and with electronic design automation (“EDA”) tool producers, including Cadence, Co-Ware and Synopsys. We also participate in joint European research programs, such as the MEDEA+ and ITEA programs, and cooperate on a global basis with major research institutions and universities. In 2007 we were a founding member of SOI (Silicon-on-Insulator) Industry Consortium.

We participated in the definition of the New Eureka program named CATRENE and to the European Nanoelectronics Initiative Advisory (“ENIAC”) programs definition.

In 2004, we signed and announced a joint venture agreement with Hynix Semiconductor to build a front-end memory-manufacturing facility in Wuxi City, China, and we plan to contribute this asset to Numonyx.

Customers and Applications

We design, develop, manufacture and market thousands of products that we sell to thousands of customers. Our major customers include Alcatel-Lucent, Bosch, Cisco, Conti, Delphi, Delta, Denso, Ericsson, Hewlett-Packard, LG Electronics, Marelli, Maxtor, Motorola, Nintendo, Nokia, Philips, Pioneer, Samsung, Seagate, Sharp, Siemens, Thomson and Western Digital. To many of our key customers we provide a wide range of products, including application-specific products, discrete devices, memory products and programmable products. Our position as a strategic supplier of application-specific products to certain customers fosters close relationships that provide us with opportunities to supply such customers’ requirements for other products, including discrete devices, programmable products and memory products. We also sell our products through distributors and retailers, including Arrow Electronics, Avnet, BSI Semiconductor, Future Electronics, Wintech and Yosun.

compete. See "Item 3. Key Information — Risk Factors — Risks Related to Our Operations — We depend on patents to protect our rights to our technology."

We record a provision when it is probable that a liability has been incurred and when the amount of the loss can be reasonably estimated. We regularly evaluate losses and claims to determine whether they need to be adjusted based on the current information available to us. Legal costs associated with claims are expensed as incurred. We are in discussion with several parties with respect to claims against us relating to possible infringements of patents and similar intellectual property rights of others.

We are currently a party to legal proceedings with SanDisk Corporation.

On October 15, 2004, SanDisk filed a complaint for patent infringement and a declaratory judgment of non-infringement and patent invalidity against us with the United States District Court for the Northern District of California. The complaint alleges that our products infringed a single SanDisk U.S. patent and seeks a declaratory judgment that SanDisk did not infringe several of our U.S. patents (Civil Case No. C 04-04379JF). By an order dated January 4, 2005, the court stayed SanDisk's patent infringement claim, pending final determination in an action filed contemporaneously by SanDisk with the United States International Trade Commission ("ITC"), which covers the same patent claim asserted in Civil Case No. C 04-04379JF. The ITC action was subsequently resolved in our favor. On August 2, 2007, SanDisk filed an amended complaint adding allegations of infringement with respect to a second SanDisk U.S. patent which had been the subject of a second ITC action and which was also resolved in our favor. On September 6, 2007, we filed an answer and a counterclaim alleging various federal and state antitrust and unfair competition claims. SanDisk filed a motion to dismiss our antitrust counterclaim, which was denied on January 25, 2008. Discovery is now proceeding.

On October 14, 2005, we filed a complaint against SanDisk and its current CEO, Dr. Eli Harari, before the Superior Court of California, County of Alameda. The complaint seeks, among other relief, the assignment or co-ownership of certain SanDisk patents that resulted from inventive activity on the part of Dr. Harari that took place while he was an employee, officer and/or director of Waferscale Integration, Inc. and actual, incidental, consequential, exemplary and punitive damages in an amount to be proven at trial. We are the successor to Waferscale Integration, Inc. by merger. SanDisk removed the matter to the United States District Court for the Northern District of California which remanded the matter to the Superior Court of California, County of Alameda in July 2006. SanDisk moved to transfer the case to the Superior Court of California, County of Santa Clara and to strike our claim for unfair competition, which were both denied by the trial court. SanDisk appealed these rulings and also moved to stay the case pending resolution of the appeal. On January 12, 2007, the California Court of Appeals ordered that the case be transferred to the Superior Court of California County of Santa Clara. On August 7, 2007, the California Court of Appeals affirmed the Superior Court's decision denying SanDisk's motion to strike our claim for unfair competition. SanDisk appealed this ruling to the California Supreme Court, which refused to hear it. Discovery is now proceeding. A hearing on Dr. Hariri's motion for summary judgment on the statute of limitations defense is scheduled for the third quarter of 2008.

With respect to the lawsuits with SanDisk as described above, and following two prior decisions in our favor taken by the ITC, we have not identified any risk of probable loss that is likely to arise out of the outstanding proceedings.

We are also a party to legal proceedings with Tessera, Inc.

On January 31, 2006, Tessera added our Company as a co-defendant, along with several other semiconductor and packaging companies, to a lawsuit filed by Tessera on October 7, 2005 against Advanced Micro Devices Inc. and Spansion in the United States District Court for the Northern District of California. Tessera is claiming that certain of our small format BGA packages infringe certain patents owned by Tessera, and that ST is liable for damages. Tessera is also claiming that various ST entities breached a 1997 License Agreement and that ST is liable for unpaid royalties as a result. In February and March 2007, our codefendants Siliconware Precision Industries Co., Ltd. and Siliconware USA, Inc., filed reexamination requests with the U.S. Patent and Trademark Office covering all of the patents and claims asserted by Tessera in the lawsuit. In April and May 2007, the U.S. Patent and Trademark Office initiated reexaminations in response to all of the reexamination requests and final decisions regarding the reexamination requests are pending. On May 24, 2007, this action was stayed pending the outcome of the ITC proceeding described below.

On April 17, 2007, Tessera filed a complaint against us, Spansion, ATI Technologies, Inc., Qualcomm, Motorola and Freescale with the ITC with respect to certain small format ball grid array packages and products containing the same, alleging patent infringement claims of two of the Tessera patents previously asserted in the District Court action described above and seeking an order excluding importation of such products into the United States. On May 15, 2007, the ITC instituted an investigation pursuant to 19 U.S.C. § 1337, entitled In the Matter of

EXHIBIT C

As filed with the Securities and Exchange Commission on May 13, 2009

SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

Form 20-F

☐ **REGISTRATION STATEMENT PURSUANT TO SECTION 12(b) OR (g) OF THE SECURITIES EXCHANGE ACT OF 1934**

OR

☑ **ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

For the fiscal year ended December 31, 2008

OR

☐ **TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

For the transition period from to

☐ **SHELL COMPANY REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

Date of event requiring this shell company report

Commission file number: 1-13546

STMicroelectronics N.V.

(Exact name of registrant as specified in its charter)

Not Applicable	**The Netherlands**
(Translation of registrant's name into English)	*(Jurisdiction of incorporation or organization)*

39, Chemin du Champ des Filles
1228 Plan-Les-Ouates
Geneva
Switzerland
(Address of principal executive offices)

Carlo Bozotti
39, Chemin du Champ des Filles
1228 Plan-Les-Ouates
Geneva
Switzerland
Tel: +41 22 929 29 29
Fax: +41 22 929 29 88
(*Name, Telephone, E-mail and/or Facsimile number and Address of Company Contact Person)*

Securities registered or to be registered pursuant to Section 12(b) of the Act:

Title of Each Class:	**Name of Each Exchange on Which Registered:**
Common shares, nominal value €1.04 per share	New York Stock Exchange

Securities registered or to be registered pursuant to Section 12(g) of the Act: None

Securities for which there is a reporting obligation pursuant to Section 15(d) of the Act: None

Indicate the number of outstanding shares of each of the issuer's classes of capital or common stock as of the close of the period covered by the annual report:

874,276,833 common shares at December 31, 2008

Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act.

Yes ☑ No ☐

If this report is an annual or transition report, indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or 15 (d) of the Securities Exchange Act of 1934.

Yes ☐ No ☑

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days:

Yes ☑ No ☐

Indicate by check mark whether the registrant has submitted electronically and posted on its corporate Web site, if any, every Interactive Data File required to be submitted and posted pursuant to Rule 405 of Regulation S-T during the preceding 12 months (or for such shorter period that the

registrant was required to submit and post such files).

Yes ☐ No ☐

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer, or a smaller reporting company. See the definitions of "large accelerated filer," "accelerated filer" and "smaller reporting company" in Rule 12b-2 of the Exchange Act. (Check one):

Large accelerated filer ☑ Accelerated filer ☐ Non-accelerated filer ☐ Smaller reporting company ☐
(Do not check if a smaller reporting company)

Indicate by check mark which basis of accounting the registrant has used to prepare the financial statements included in this filing:

U.S. GAAP ☑ International Financial Reporting Standards as issued by the International Accounting Standards Board ☐ Other ☐

If "Other" has been checked in response to the previous question, indicate by check mark which financial statement item the registrant has elected to follow.

Item 17 ☐ Item 18 ☐

If this is an annual report, indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Exchange Act).

Yes ☐ No ☑

to improve our cost structure and competitiveness in the semiconductor market, such as seeking more competitive sources of production, discontinuing certain product families or performing additional restructurings, which in turn may result in loss of revenues, asset impairments and/or capital losses.

Risks Related to Our Operations

Market dynamics are driving us to a strategic repositioning, which has led us to enter into significant joint ventures.

As a result of a strategic review of our product portfolio, in 2008 we divested our Flash Memory activities by combining our business with that of Intel and creating Numonyx, a new independent semiconductor company in the area of Flash memories. The intent is that Numonyx will benefit from critical size to be competitive in this market. The transaction concerning the creation of Numonyx closed on March 30, 2008. We incurred a total impairment and disposal loss of $1,297 million in connection with this transaction, of which $190 million was recorded in the year ended December 31, 2008, and $31 million of other restructuring charges, of which $26 million was incurred in the year ended December 31, 2008. We also incurred losses in 2008 related to our equity holding in Numonyx, for a total amount of approximately $545 million, including a $480 million impairment on the equity investment. In the first quarter of 2009, we also incurred losses of $229 million, out of which $200 million was an additional impairment on the equity investment in Numonyx. There is no assurance that if the flash memory market were to further deteriorate, or if Numonyx were unable to effectively compete or maintain its market position, Numonyx will not be required to undertake further restructurings, which in turn could lead to additional impairments and associated charges.

We also recently undertook new initiatives to reposition our business. In January 2008, we completed the acquisition of Genesis Microchip Inc. (“Genesis Microchip”) for $340 million and in August 2008, we completed the acquisition of NXP’s wireless business for $1,550 million, creating the joint venture, ST-NXP Wireless. Furthermore, in February 2009, we completed the merger of ST-NXP Wireless with EMP, thereby forming ST-Ericsson and in connection therewith we purchased the outstanding 20% held by NXP’s ST-NXP Wireless for a price of $92 million. The wireless activities run through ST-Ericsson represent a significant portion of our business. The integration process may be long and complex due to the fact that we are merging three different companies. On April 29, 2009, ST-Ericsson announced a restructuring plan giving rise to costs estimated in the range of $70 million to $90 million. We may not be able to exercise the same control over management as we did when the business was operated by us. There is no assurance that we will be successful or that the joint venture will produce the planned operational and strategic benefits.

We are constantly monitoring our product portfolio and cannot exclude that additional steps in this repositioning process may be required; further, we cannot assure that any strategic repositioning of our business, including possible future acquisitions, dispositions or joint ventures, will be successful and may not result in further impairment and associated charges.

Future acquisitions or divestitures may adversely affect our business.

Our strategies to improve our results of operations and financial condition may lead us to make significant acquisitions of businesses that we believe to be complementary to our own, or to divest ourselves of activities that we believe do not serve our longer term business plans. In addition, certain regulatory approvals for potential acquisitions may require the divestiture of business activities.

Our potential acquisition strategies depend in part on our ability to identify suitable acquisition targets, finance their acquisition and obtain required regulatory and other approvals. Our potential divestiture strategies depend in part on our ability to define the activities in which we should no longer engage, and then determine and execute appropriate methods to divest of them.

Acquisitions and divestitures involve a number of risks that could adversely affect our operating results, including the risk that we may be unable to successfully integrate businesses or teams we acquire with our culture and strategies on a timely basis or at all, and the risk that we may be required to record charges related to the goodwill or other long-term assets associated with the acquired businesses. Changes in our expectations due to changes in market developments that we cannot foresee have in the past resulted in our writing off amounts

EXHIBIT D

As filed with the Securities and Exchange Commission on March 10, 2010

SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

Form 20-F

☐ **REGISTRATION STATEMENT PURSUANT TO SECTION 12(b) OR (g) OF THE SECURITIES EXCHANGE ACT OF 1934**

OR

☑ **ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

For the fiscal year ended December 31, 2009

OR

☐ **TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

For the transition period from to

☐ **SHELL COMPANY REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

Date of event requiring this shell company report

Commission file number: 1-13546

STMicroelectronics N.V.

(Exact name of registrant as specified in its charter)

Not Applicable	**The Netherlands**
(Translation of registrant's name into English)	*(Jurisdiction of incorporation or organization)*

39, Chemin du Champ des Filles
1228 Plan-Les-Ouates
Geneva
Switzerland
(Address of principal executive offices)

Carlo Bozotti
39, Chemin du Champ des Filles
1228 Plan-Les-Ouates
Geneva
Switzerland
Tel: +41 22 929 29 29
Fax: +41 22 929 29 88
(Name, Telephone, E-mail and/or Facsimile number and Address of Company Contact Person)

Securities registered or to be registered pursuant to Section 12(b) of the Act:

Title of Each Class:	**Name of Each Exchange on Which Registered:**
Common shares, nominal value 1.04 per share	New York Stock Exchange

Securities registered or to be registered pursuant to Section 12(g) of the Act: None
Securities for which there is a reporting obligation pursuant to Section 15(d) of the Act: None

Indicate the number of outstanding shares of each of the issuer's classes of capital or common stock as of the close of the period covered by the annual report:

878,333,566 common shares at December 31, 2009

Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act.

Yes ☑ No ☐

If this report is an annual or transition report, indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or 15(d) of the Securities Exchange Act of 1934.

Yes ☐ No ☑

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days:

Yes ☑ No ☐

Indicate by check mark whether the registrant has submitted electronically and posted on its corporate Web site, if any, every Interactive Data File required to be submitted and posted pursuant to Rule 405 of Regulation S-T during the preceding 12 months (or for such shorter period that the registrant was required to submit and post such files).

Yes ☑ No ☐

on our Numonyx equity investment, a $32 million loss related to our proportionate share in JVD as a loss pick-up including an amortization of basis difference and $2 million related to other investments.

In 2008, our income on equity investments included our minority interest in the joint venture with Hynix Semiconductor in China, which was transferred to Numonyx on March 30, 2008.

Gain (loss) on financial assets

	Year Ended December 31,	
	2009	2008
	(Audited, in millions)	
Gain (loss) on financial assets	$(8)	$15

In 2006, we entered into cancellable swaps with a combined notional value of $200 million to hedge the fair value of a portion of the convertible bonds due 2016 carrying a fixed interest rate. The cancellable swaps convert the fixed rate interest expense recorded on the convertible bonds due 2016 to a variable interest rate based upon adjusted LIBOR. Until November 1, 2008, the cancellable swaps met the criteria for designation as a fair value hedge. Due to the exceptionally low U.S. dollar interest rate as a consequence of the financial crisis, we assessed in 2008 that the swaps were no longer effective as of November 1, 2008 and the fair value hedge relationship was discontinued. Consequently, the swaps were classified as held-for-trading financial assets. An unrealized gain of $15 million was recognized in earnings from the discontinuance date and was reported on the line "Unrealized gain on financial assets" in the consolidated statement of income for the year ended December 31, 2008.

This instrument was sold in 2009 with a loss of $8 million due to variation in the underlying interest rates compared to December 31, 2008.

Gain on convertible debt buyback

	Year Ended December 31,	
	2009	2008
	(Audited, In millions)	
Gain on convertible debt buyback	$3	$—

The $3 million gain on convertible debt buyback is related to the repurchase of bonds with a principal value of $106 million for total cash consideration of $103 million. Please see "Capital Resources".

Income tax benefit

	Year Ended December 31,	
	2009	2008
	(Audited, in millions)	
Income tax benefit	$95	$43

In 2009, we registered an income tax benefit of $95 million, reflecting the actual tax benefit estimated on our loss before income taxes in each of our jurisdictions. This benefit was net of about $56 million booked as a tax expense related to the valuation allowances on our deferred tax asset associated with our estimates of the net operating loss recoverability in certain jurisdictions.

Net loss (income) attributable to noncontrolling interest

	Year Ended December 31,	
	2009	2008
	(Audited, in millions)	
Net loss (income) attributable to noncontrolling interest	$270	$ (6)
As a percentage of net revenues	3.2%	(0.1)%

In 2009, we booked $270 million in income, which primarily represented the share of the loss attributable to noncontrolling interest that included the 20% owned by NXP in the ST-NXP joint venture for the month of January 2009 and the 50% owned by Ericsson in the consolidated ST-Ericsson Holding AG as of February 2009. This amount reflected their share in the joint venture's losses.

EXHIBIT E

UNITED STATES SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

FORM 6-K

REPORT OF FOREIGN PRIVATE ISSUER
PURSUANT TO RULE 13a-16 OR 15d-16 UNDER
THE SECURITIES EXCHANGE ACT OF 1934

Report on Form 6-K dated August 3, 2010

Commission File Number: 1-13546

STMicroelectronics N.V.

(Name of Registrant)

39, Chemin du Champ-des-Filles
1228 Plan-les-Ouates, Geneva, Switzerland
(Address of Principal Executive Offices)

Indicate by check mark whether the registrant files or will file annual reports under cover of Form 20-F or Form 40-F:

Form 20-F ☒ Form 40-F ☐

Indicate by check mark if the registrant is submitting the Form 6-K in paper as permitted by Regulation S-T Rule 101(b)(1):

Yes ☐ No ☒

Indicate by check mark if the registrant is submitting the Form 6-K in paper as permitted by Regulation S-T Rule 101(b)(7):

Yes ☐ No ☒

Indicate by check mark whether the registrant by furnishing the information contained in this form is also thereby furnishing the information to the Commission pursuant to Rule 12g3-2(b) under the Securities Exchange Act of 1934:

Yes ☐ No ☒

If "Yes" is marked, indicate below the file number assigned to the registrant in connection with Rule 12g3-2(b): 82-_____

Enclosure: STMicroelectronics N.V.'s Second Quarter and First Half 2010:

- Operating and Financial Review and Prospects;
- Unaudited Interim Consolidated Statements of Income, Balance Sheets, Statements of Cash Flow, and Statements of Changes in Equity and related Notes for the three months and six months ended June 26, 2010; and
- Certifications pursuant to Sections 302 (Exhibits 12.1 and 12.2) and 906 (Exhibit 13.1) of the Sarbanes-Oxley Act of 2002, submitted to the Commission on a voluntary basis.

Fiscal Year

Under Article 35 of our Articles of Association, our financial year extends from January 1 to December 31, which is the period end of each fiscal year. The first and second quarters of 2010 ended on March 27 and June 26, 2010, respectively. The third quarter of 2010 will end on September 25 and the fourth quarter will end on December 31, 2010. Based on our fiscal calendar, the distribution of our revenues and expenses by quarter may be unbalanced due to a different number of days in the various quarters of the fiscal year.

Business Overview

The total available market is defined as the "TAM", while the serviceable available market, the "SAM", is defined as the market for products produced by us (which consists of the TAM and excludes PC motherboard major devices such as Microprocessors ("MPUs"), dynamic random access memories ("DRAMs"), optoelectronics devices and Flash Memories).

The growth momentum of the semiconductor industry continued during the second quarter of 2010, characterized by strong demand in almost all market applications, which led to total revenues reaching a high quarterly level. As a result, on year-over-year and sequential basis, the second quarter registered a solid performance. Based on published industry data by WSTS, semiconductor industry revenues increased in the second quarter of 2010 by approximately 43% for the TAM and 31% for the SAM on a year-over-year basis to reach approximately $75 billion and $42 billion, respectively. On a sequential basis, TAM and SAM registered an increase of approximately 7% and 6%, respectively.

With reference to our business performance, during the second quarter of 2010 we continued to register strong demand from our customers, which translated in a higher level of both orders and revenues. Revenues increased to $2,531 million, a 27.0% increase over the same period in 2009, led by the ACCI and IMS product segments, while Wireless revenues decreased. On a year-over-year basis our overall performance result was below the SAM.

On a sequential basis, our second quarter 2010 revenues increased 8.9%, in line with our anticipated guidance, still driven by ACCI and IMS. Our sequential performance was above the SAM.

Our effective average exchange rate for the first half of 2010 was $1.37 for €1.00 compared to $1.33 for €1.00 for the first half of 2009. Our effective average exchange rate for the second quarter of 2010 was $1.35 for €1.00 compared to $1.39 for €1.00 for the first quarter of 2010 and $1.34 for €1.00 in the second quarter of 2009. For a more detailed discussion of our hedging arrangements and the impact of fluctuations in exchange rates, see "Impact of Changes in Exchange Rates" below.

Our second quarter 2010 gross margin was 38.3%, largely improving compared to the 26.1% registered in the year-ago period. The second quarter of 2010 benefited from the favorable impact of several factors, including (i) a more favorable industry environment, which contributed to improved sales volume and, consequently, the loading of our fabs; and (ii) overall improvement in our manufacturing efficiencies resulting from our restructuring and cost cutting measures, in particular the closing of certain fabs. However, the second quarter of 2009 was largely penalized by significant unused capacity charges associated with poor loading, accounting for approximately 6 percentage points. Sequentially, our gross margin improved 60 basis points, mainly due to higher volume, product mix improvements in both ACCI and IMS and the recognition of a technology licensing arrangement in other revenues.

Our second quarter 2010 operating result rebounded from several quarters of operating losses to reach a solid profit level. The second quarter 2010 result was an operating income of $91 million, a significant improvement compared to the $428 million loss in the second quarter of 2009, driven by higher revenues, as well as overall improvement of our manufacturing performance and control of our operating expenses. Our second quarter 2010 operating income improved sequentially from a $20 million loss in the first quarter of 2010, mainly due to higher revenues. The strengthening U.S. dollar exchange rate had a non material impact on our second quarter 2010 financial result. See "Impact of Changes in Exchange Rates".

The second quarter of 2010 includes the exceptional gain of $265 million on the Numonyx equity divestiture, for which we received shares of Micron common stock, evaluated at $583 million at closing, as compensation.

As we did in the first half of 2010, we continue to increase capacity to support the strong demand of our customers and are encouraged by the quality of our backlog.

In addition, we made significant progress during the first half of 2010 with respect to enhancing our product portfolio, improving our financial performance and strengthening our financial position. Looking ahead to the second half of the year, we expect to see further positive progression in our performance.

This outlook is based on an assumed effective currency exchange rate of approximately $1.32 = €1.00 for the 2010 third quarter, which reflects an assumed exchange rate of $1.23 = €1.00 combined with the impact of existing hedging contracts. The third quarter will close on September 25, 2010.

These are forward-looking statements that are subject to known and unknown risks and uncertainties that could cause actual results to differ materially; in particular, refer to those known risks and uncertainties described in "Cautionary Note Regarding Forward-Looking Statements" herein and "Item 3. Key Information—Risk Factors" in our Form 20-F as may be updated from time to time in our SEC filings.

Other Developments

On January 4, 2010, we signed a joint agreement with Enel and Sharp for the manufacture of triple-junction thin-film photovoltaic panels in Italy. On August 2, 2010, we announced, together with Enel and Sharp, the signature of a binding commitment letter for a €150 million project financing agreement and our equal share joint venture, named 3Sun, began operations at the Catania, Italy factory. The Catania factory's initial photovoltaic panel production capacity, equivalent to 160 MW per year, is to be financed through a combination of self-financing, funding from the Italian Joint Ministerial Committee for Economic planning, which recently committed €49 million to this project, and project financing provided by leading banks. We, Enel and Sharp have each underwritten one third of the joint venture's equity, with a commitment of €70 million in cash or in tangible and intangible assets, and hold one third of its shares. Our equity commitment will be satisfied by the contribution of the M6 facility in Catania (see below) for a value of €60 million and a €10 million cash contribution. Panel production at the Catania plant is scheduled to begin in the second half of 2011.

On February 3, 2010, we announced that Tjerk Hooghiemstra joined us as Executive Vice-President, Chief Administrative Officer, reporting to our President and CEO, Carlo Bozotti. This new position was created with the aim of generating synergies among several staff organizations by optimizing the functions of Human Resources, Health & Safety, Education, Legal, Internal Communication, Security and Corporate Responsibility.

Numonyx

On February 10, 2010, we, together with our partners Intel Corporation and Francisco Partners, entered into a definitive agreement with Micron Technology Inc., in which Micron would acquire Numonyx Holdings B.V. in an all-stock transaction. On May 7, 2010, this transaction closed. In exchange for our 48.6% stake in Numonyx, we received approximately 66.88 million shares of Micron common stock, which is recorded as a financial investment. At the May 6, 2010 Micron closing share price of $8.75 per share, the value of the shares was $585.2 million. Due to the high volatility in the share price, the value of these shares could be subject to material variations and, therefore, in order to partially protect the value of the transaction, we have hedged, with certain derivative instruments, a significant portion of the 66.88 million shares. For the details of these hedging operations, refer to Note 27 to our Unaudited Interim Consolidated Financial Statements. We also have a payable of $78 million, equivalent to 10 million shares of Micron common stock, due to Francisco Partners at the end of the shares' six month lock-up period. Also, at the closing of this transaction, the senior credit facility that was supported by our guarantee of $225 million was repaid in full by Numonyx. The overall transaction results in a gain after tax of approximately $265 million, higher than the amount previously announced, which is reported in our fiscal second quarter Consolidated Statement of Income. In connection with the divestiture of Numonyx we also received full ownership of the Numonyx M6 facility in Catania, Italy, which, as noted above, we are contributing to 3Sun, the new photovoltaic joint initiative among Enel, Sharp and us.

Under the terms of the agreement to sell Numonyx to Micron, we continue to retain the $250 million deposit with DBS Bank Ltd. in Singapore, which is intended to guarantee the Hynix-Numonyx Joint Venture's debt financing for

EXHIBIT F

UNITED STATES
SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

FORM 8-K

CURRENT REPORT
Pursuant to Section 13 OR 15(d) of The Securities Exchange Act of 1934

May 7, 2010
Date of Report (date of earliest event reported)

MICRON TECHNOLOGY, INC.
(Exact name of registrant as specified in its charter)

Delaware	**1-10658**	**75-1618004**
(State or other jurisdiction of incorporation)	(Commission File Number)	(I.R.S. Employer Identification No.)

8000 South Federal Way
Boise, Idaho 83716-9632
(Address of principal executive offices)

(208) 368-4000
(Registrant's telephone number, including area code)

Check the appropriate box below if the Form 8-K filing is intended to simultaneously satisfy the filing obligation of the registrant under any of the following provisions (see General Instruction A.2. below):

☐ Written communications pursuant to Rule 425 under the Securities Act (17 CFR 230.425)

☐ Soliciting material pursuant to Rule 14a-12 under the Exchange Act (17 CFR 240.14a-12)

☐ Pre-commencement communications pursuant to Rule 14d-2(b) under the Exchange Act (17 CFR 240.14d-2(b))

☐ Pre-commencement communications pursuant to Rule 13e-4(c) under the Exchange Act (17 CFR 240.13e-4c))

EXHIBIT 99.1

FOR IMMEDIATE RELEASE

Contacts:

Kipp A. Bedard	Daniel Francisco
Investor Relations	Media Relations
kbedard@micron.com	dfrancisco@micron.com
(208) 368-4465	(208) 368-5584

MICRON ANNOUNCES CLOSING OF NUMONYX ACQUISITION

Micron Offers One of Most Comprehensive, Cost-Competitive Memory Product Portfolios in Industry with Numonyx Acquisition

BOISE, Idaho, and GENEVA, May 7, 2010 – Micron Technology, Inc., (NASDAQ: MU) announced today that the company has completed its acquisition of Numonyx B.V. in an all stock transaction valued at approximately $1.2 billion USD. Under the agreement, Micron issued approximately 138 million shares of Micron common stock to Numonyx shareholders, Intel, STMicroelectronics, N.V. and Francisco Partners, and assumed outstanding restricted stock units held by Numonyx employees.

“With this acquisition, Micron builds on its position as one of the world’s leading memory companies with increased scale, a broader product portfolio and industry-leading technology,” said Steve Appleton, Chairman and CEO of Micron.

The transaction further strengthens Micron’s broad portfolio of DRAM, NAND and NOR memory products and strong expertise in developing and supporting memory system solutions. Micron also gains increased manufacturing and revenue scale along with access to Numonyx’s customer base, providing significant opportunities to increase multi-chip offerings in the embedded and mobile markets.

As of Dec. 31, 2009, Numonyx reported net assets of $1.3 billion and cash and cash equivalents, net of debt to unrelated parties of $70 million. In the fourth calendar quarter, Numonyx generated $42 million in free cash flow based on quarterly revenues of approximately $550 million.

About Micron
Micron Technology, Inc., is one of the world's leading providers of advanced semiconductor solutions. Through its worldwide operations, Micron manufactures and markets a full range of DRAM, NAND and NOR flash memory, as well as other innovative memory technologies, packaging solutio semiconductor systems for use in leading-edge computing, consumer, networking, embedded and mobile products. Micron’s common stock is traded NASDAQ under the MU symbol. To learn more about Micron Technology, Inc., visit www.micron.com.

###

This press release contains forward-looking statements regarding the impact of the acquisition on Micron’s results and operations. Actual events or results may differ materially from those contained in the forward-looking statements. Please refer to the documents Micron files on a consolidated basis from time to time with the Securities and Exchange Commission, specifically Micron's most recent Form 10-K and Form 10-Q. These documents contain and identify important factors that could cause the actual results for Micron on a consolidated basis to differ materially from those contained in our forward-looking statements (see Certain Factors). Although we believe that the expectations reflected in the forward-looking statements are reasonable, we cannot guarantee future results, levels of activity, performance or achievements.

EXHIBIT G

SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

FORM 6-K

REPORT OF FOREIGN PRIVATE ISSUER
PURSUANT TO RULE 13a-16 or 15d-16 OF
THE SECURITIES EXCHANGE ACT OF 1934

Report on Form 6-K dated May 4, 2005

STMicroelectronics N.V.

(Name of Registrant)

39, Chemin du Champ-des-Filles
1228 Plan-les-Ouates, Geneva, Switzerland
(Address of Principal Executive Offices)

Indicate by check mark whether the registrant files or will file annual reports under cover of Form 20-F or Form 40-F:

Form 20-F ☒ Form 40-F ☐

Indicate by check mark if the registrant is submitting the Form 6-K in paper as permitted by Regulation S-T Rule 101(b)(7):

Yes ☐ No ☒

Indicate by check mark whether the registrant by furnishing the information contained in this form is also thereby furnishing the information to the Commission pursuant to Rule 12g3-2(b) under the Securities Exchange Act of 1934:

Yes ☐ No ☒

If "Yes" is marked, indicate below the file number assigned to the registrant in connection with Rule 12g3-2(b): 82- _____

Enclosure: STMicroelectronics N.V.'s First Quarter 2005:

- Operating and Financial Review and Prospects;
- Unaudited Interim Consolidated Statements of Income, Balance Sheets, Statements of Cash Flow, and Statements of Changes in Shareholders' Equity and related Notes for the three months ended April 2, 2005; and
- Certifications pursuant to Sections 302 (Exhibits 12.1 and 12.2) and 906 (Exhibit 13.1) of the Sarbanes-Oxley Act of 2002, submitted to the Commission on a voluntary basis.

Back to Contents

As of April 2, 2005, none of the common shares repurchased had been transferred to employees under the employee stock option plan.

18. Contingencies

The Company is subject to the possibility of loss contingencies arising in the ordinary course of business. These include but are not limited to: warranty cost on the products of the Company not covered by insurance, breach of contract claims, claims for unauthorized use of third party intellectual property, tax claims and provisions for specifically identified income tax exposures as well as claims for environmental damages. In determining loss contingencies, the Company considers the likelihood of a loss of an asset or the incurrence of a liability as well as the ability to reasonably estimate the amount of such loss or liability. An estimated loss is recorded when it is probable that a liability has been incurred and when the amount of the loss can be reasonably estimated. The Company regularly reevaluates claims to determine whether provisions need to be readjusted based on the most current information available to the Company. Adverse changes in evaluations which result in adverse determinations with respect to the interests of the Company could have a material negative effect on the Company's results of operations, cash flows or its financial position for the period in which they occur.

19. Claims and Legal proceedings

The Company has received and may in the future receive communications alleging possible infringements, in particular in the case of patents and similar intellectual property rights of others. Furthermore, the Company may become involved in costly litigation brought against the Company regarding patents, mask works, copyrights, trademarks or trade secrets. In the event that the outcome of any litigation would be unfavorable to the Company, the Company may be required to license the underlying intellectual property right at economically unfavorable terms and conditions, and possibly pay damages for prior use and/or face an injunction, all of which individually or in the aggregate could have a material adverse effect on the Company's results of operations, cash flows or financial position and ability to compete.

The Company is involved in various lawsuits, claims, investigations and proceedings incidental to the normal conduct of its operations, other than external patent utilization. These matters mainly include the risks associated with claims from customers or other parties and tax disputes. The Company has accrued for these loss contingencies when the loss is probable and can be estimated. The Company regularly evaluates claims and legal proceedings together with their related probable losses to determine whether they need to be adjusted based on the current information available to the Company. Legal costs associated with claims are expensed as incurred. In the event of litigation which is adversely determined with respect to the Company's interests, or in the event the Company needs to change its evaluation of a potential third-party claim, based on new evidence or communications, a material adverse effect could impact its operations or financial condition at the time it were to materialize.

During 2004, the Company has settled certain disputes with respect to claims and litigation relating to possible infringements of patents and similar intellectual property rights of others. An accrual of $10 million had been established at December 31, 2003 for such claims, which was paid in the first quarter of 2005 in accordance with the final settlements. No additional accrual has been recorded in 2005 since no other risks were estimated to result in a probable loss.

The Company is currently a party to legal proceedings with SanDisk Corporation ("SanDisk"). Based on management's current assumptions made with support of the company's outside attorneys, the Company does not believe that the SanDisk litigation will result in a probable loss.

EXHIBIT H

UNITED STATES SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

FORM 6-K

REPORT OF FOREIGN PRIVATE ISSUER
PURSUANT TO RULE 13a-16 OR 15d-16 UNDER
THE SECURITIES EXCHANGE ACT OF 1934

Report on Form 6-K dated May 19, 2009

Commission File Number: 1-13546

STMicroelectronics N.V.

(Name of Registrant)

39, Chemin du Champ-des-Filles
1228 Plan-les-Ouates, Geneva, Switzerland
(Address of Principal Executive Offices)

Indicate by check mark whether the registrant files or will file annual reports under cover of Form 20-F or Form 40-F:

Form 20-F Q Form 40-F £

Indicate by check mark if the registrant is submitting the Form 6-K in paper as permitted by Regulation S-T Rule 101(b)(1):

Yes £ No Q

Indicate by check mark if the registrant is submitting the Form 6-K in paper as permitted by Regulation S-T Rule 101(b)(7):

Yes £ No Q

Indicate by check mark whether the registrant by furnishing the information contained in this form is also thereby furnishing the information to the Commission pursuant to Rule 12g3-2(b) under the Securities Exchange Act of 1934:

Yes £ No Q

If "Yes" is marked, indicate below the file number assigned to the registrant in connection with Rule 12g3-2(b): 82- _____

Enclosure: STMicroelectronics N.V.'s First Quarter 2009:

- Operating and Financial Review and Prospects;
- Unaudited Interim Consolidated Statements of Income, Balance Sheets, Statements of Cash Flow, and Statements of Changes in Equity and related Notes for the three months ended March 28, 2009; and
- Certifications pursuant to Sections 302 (Exhibits 12.1 and 12.2) and 906 (Exhibit 13.1) of the Sarbanes-Oxley Act of 2002, submitted to the Commission on a voluntary basis.

We also present our pro forma earnings (loss) per share, calculated by adding back to net income (loss) attributable to parent company, as reported, our impairment and restructuring charges and, when applicable, other one-time items. We believe pro forma earnings (loss) per share provide useful information for investors and management because they measure our capacity to generate earnings from our business operations, excluding the expenses related to the rationalizing of our activities and sites and the one-time effects of acquisitions. Pro forma earnings (loss) per share are not a U.S. GAAP measure and do not fully present our earnings (loss) per share attributable to parent company since they do not include impairment and restructuring charges and other items related to purchase accounting, when applicable.

In the first quarter of 2009, the impact of restructuring and impairment charges, other-than-temporary impairment charges and the loss on our Numonyx equity investment was estimated to be approximately $(0.31) per share. In the fourth quarter of 2008, loss per share was impacted for approximately $(0.36) per share by restructuring and impairment charges, other-than-temporary impairment charges, the loss on our Numonyx equity investment and non-recurring items. In the year-ago quarter, the impact of impairment, restructuring and other-than temporary impairment charges was estimated to be equivalent to approximately $(0.22) per share.

Legal Proceedings

As is the case with many companies in the semiconductor industry, we have from time to time received, and may in the future receive, communications from other semiconductor companies or third parties alleging possible infringement of patents. Furthermore, we may become involved in costly litigation brought against us regarding patents, copyrights, trademarks, trade secrets or mask works. In the event the outcome of any litigation is unfavorable to us, we may be required to take a license to the underlying intellectual property right upon economically unfavorable terms and conditions, and possibly pay damages for prior use, and/or face an injunction, all of which individually or in the aggregate could have a material adverse effect on our results of operations and ability to compete. See “Item 3. Key Information — Risk Factors — Risks Related to Our Operations — We depend on patents to protect our rights to our technology.”

We record a provision when it is probable that a liability has been incurred and when the amount of the loss can be reasonably estimated. We regularly evaluate losses and claims to determine whether they need to be adjusted based on the current information available to us. Legal costs associated with claims are expensed as incurred. We are in discussion with several parties with respect to claims against us relating to possible infringements of patents and similar intellectual property rights of others.

We are currently a party to legal proceedings with SanDisk Corporation.

On October 15, 2004, SanDisk filed a complaint for patent infringement and a declaratory judgment of non-infringement and patent invalidity against us with the United States District Court for the Northern District of California. The complaint alleged that our products infringed on a single SanDisk U.S. patent (Civil Case No. C 04-04379JF). By an order dated January 4, 2005, the court stayed SanDisk’s patent infringement claim, pending final determination in an action filed contemporaneously by SanDisk with the U.S. International Trade Commission (“ITC”), which covered the same patent claim asserted in Civil Case No. C 04-04379JF. The ITC action was subsequently resolved in our favor. On August 2, 2007, SanDisk filed an amended complaint in the United States District Court for the Northern District of California adding allegations of infringement with respect to a second SanDisk U.S. patent which had been the subject of a second ITC action and which was also resolved in our favor. On September 6, 2007, we filed an answer and a counterclaim alleging various federal and state antitrust and unfair competition claims. SanDisk filed a motion to dismiss our antitrust counterclaim, which was denied on January 25, 2008. On October 17, 2008, the Court issued an order granting in part and denying in part a summary judgment motion filed by SanDisk with respect to our antitrust counterclaims. Discovery is ongoing. SanDisk recently moved to add two additional related patents to the case. Such motion is currently pending. The trial date has not yet been set.

On October 14, 2005, we filed a complaint against SanDisk and its current CEO, Dr. Eli Harari, before the Superior Court of California, County of Alameda. The complaint seeks, among other relief, the assignment or co-ownership of certain SanDisk patents that resulted from inventive activity on the part of Dr. Harari that took place while he was an employee, officer and/or director of Waferscale Integration, Inc. and actual, incidental, consequential, exemplary

and punitive damages in an amount to be proven at trial. We are the successor to Waferscale Integration, Inc. by merger. SanDisk removed the matter to the United States District Court for the Northern District of California, which remanded the matter to the Superior Court of California, County of Alameda in July 2006. SanDisk moved to transfer the case to the Superior Court of California, County of Santa Clara and to strike our claim for unfair competition, which were both denied by the trial court. SanDisk appealed these rulings and also moved to stay the case pending resolution of the appeal. On January 12, 2007, the California Court of Appeals ordered that the case be transferred to the Superior Court of California, County of Santa Clara. On August 7, 2007, the California Court of Appeals affirmed the Superior Court's decision denying SanDisk's motion to strike our claim for unfair competition. SanDisk appealed this ruling to the California Supreme Court, which refused to hear it. On August 26, 2008, the federal court granted our motion to remand the case back to Santa Clara County and, subsequently, on September 9, 2008 SanDisk's motion for reconsideration. The case has now been re-certified in the state court and a trial date of September 8, 2009 has been set. Discovery is ongoing. In April 2009, the Court denied Sandisk's motion for summary judgement on SanDisk's affirmative defense of statute of limitations.

With respect to the lawsuits with SanDisk as described above, and following two prior decisions in our favor taken by the ITC, we have not identified any risk of probable loss that is likely to arise out of the outstanding proceedings.

We are also a party to legal proceedings with Tessera, Inc.

On January 31, 2006, Tessera added our Company as a co-defendant, along with several other semiconductor and packaging companies, to a lawsuit filed by Tessera on October 7, 2005 against Advanced Micro Devices Inc. and Spansion in the United States District Court for the Northern District of California. Tessera is claiming that certain of our small format BGA packages infringe certain patents owned by Tessera, and that we are liable for damages. Tessera is also claiming that various ST entities breached a 1997 License Agreement and that we are liable for unpaid royalties as a result. In April and May 2007, the United States Patent and Trademark Office ("PTO") initiated reexaminations in response to the reexamination requests. A final decision regarding the reexamination requests is pending.

On April 17, 2007, Tessera filed a complaint against us, Spansion, ATI Technologies, Inc., Qualcomm, Motorola and Freescale with the ITC with respect to certain small format ball grid array packages and products containing the same, alleging patent infringement claims of two of the Tessera patents previously asserted in the District Court action described above and seeking an order excluding importation of such products into the United States. On May 15, 2007, the ITC instituted an investigation pursuant to 19 U.S.C. § 1337, entitled "In the Matter of Certain Semiconductor Chips with Minimized Chip Package Size and Products Containing Same", Inv. No. 337-TA-605. The PTO's Central Reexamination Unit has issued office actions rejecting all of the asserted patent claims on the grounds that they are invalid in view of certain prior art. Tessera is contesting these rejections, and the PTO has not made a final decision. On February 25, 2008, the administrative law judge issued an initial determination staying the ITC proceeding pending completion of these reexamination proceedings. On March 28, 2008, the ITC reversed the administrative law judge and ordered him to reinstate the ITC proceeding. Trial proceedings took place from July 14, 2008 to July 18, 2008. On December 1, 2008, the ITC Administration Law Judge issued this initial determination finding the "326" and "419" patents valid but not infringed. Tessera has appealed this ruling to the ITC which, on March 26, 2009 decided to extend the deadline for completing its review and rendering its final determination until May 20, 2009. Pursuant to its review, the ITC can affirm, modify or reverse the initial determination, in whole or in part. The two Tessera patents asserted in the proceedings will expire in 2010.

In addition, in April 2008, we, along with several other companies such as Freescale, NXP Semiconductor, Grace Semiconductor, National Semiconductor, Spansion and Elpida, were sued by LSI Corp. and its wholly-owned subsidiary Agere Systems, Inc. (collectively "LSI") before the ITC in Washington, D.C. The lawsuit follows LSI Corp.'s purchase of Agere Systems Inc. and alleges infringement of a single Agere U.S. process patent (US 5,227,335). LSI is seeking an exclusion order preventing the importation into the United States of semiconductor integrated devices and products made by the methods alleged to infringe the asserted patent. The Administrative Law Judge assigned to the case set a July 2009 trial date with an initial determination on the merits due September 21, 2009. The ITC's final determination is currently scheduled for January 21, 2010. The LSI patent in suit expires July 13, 2010. A claim for patent infringement was also made by LSI in the United States District Court for the Eastern District of Texas regarding the same patent. The action in the United States District Court for the Eastern

EXHIBIT I

US005172338A

United States Patent [19]

Mehrotra et al.

[11] Patent Number: 5,172,338

[45] Date of Patent: Dec. 15, 1992

[54] **MULTI-STATE EEPROM READ AND WRITE CIRCUITS AND TECHNIQUES**

[75] Inventors: **Sanjay Mehrotra**, Milpitas; **Eliyahou Harari**, Los Gatos; **Winston Lee**, San Francisco, all of Calif.

[73] Assignee: **Sundisk Corporation**, Santa Clara, Calif.

[21] Appl. No.: **508,273**

[22] Filed: **Apr. 11, 1990**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 337,579, Apr. 13, 1989.

[51] **Int. Cl.**[5] **G11C 7/00**; G11C 29/00; G11C 16/04

[52] **U.S. Cl.** **365/185**; 365/201; 365/184; 365/195; 365/189.07

[58] **Field of Search** 365/168, 184, 185, 189.01, 365/189.07, 189.09, 201, 228, 104, 195; 371/21.4

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,253,059	2/1981	Bell et al.	371/21.4
4,460,982	7/1984	Gee et al.	371/21.4 X
4,612,629	9/1986	Harari	365/185
4,733,394	3/1988	Giebel	365/201 X
4,752,929	6/1988	Kantz et al.	371/21
4,779,272	10/1988	Kohda et al.	365/201 X
4,799,195	1/1989	Iwahashi et al.	365/185
4,809,231	2/1989	Shannon et al.	365/201
4,870,618	9/1989	Iwashita	365/201

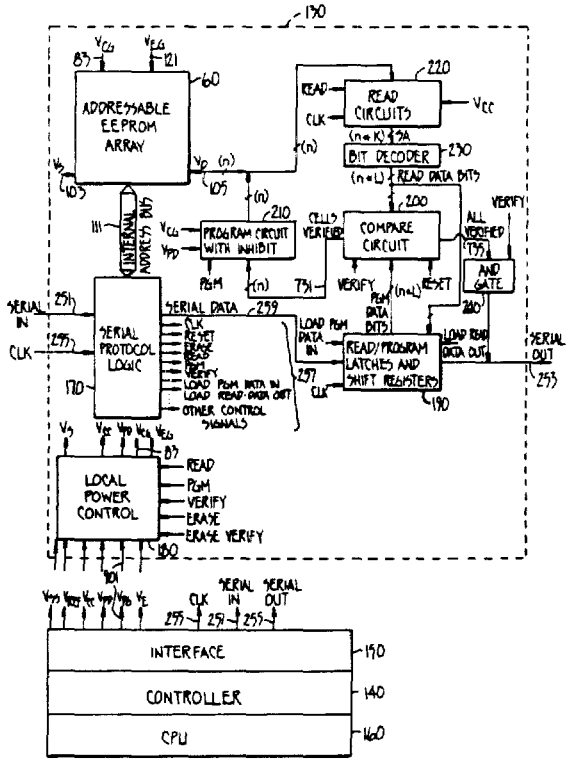
Primary Examiner—Alyssa H. Bowler

Attorney, Agent, or Firm—Majestic, Parsons, Siebert & Hsue

[57] **ABSTRACT**

Improvements in the circuits and techniques for read, write and erase of EEprom memory enable non-volatile multi-state memory to operate with enhanced performance over an extended period of time. In the improved circuits for normal read, and read between write or erase for verification, the reading is made relative to a set of threshold levels as provided by a corresponding set of reference cells which closely track and make adjustment for the variations presented by the memory cells. In one embodiment, each Flash sector of memory cells has its own reference cells for reading the cells in the sector, and a set of reference cells also exists for the whole memory chip acting as a master reference. In another embodiment, the reading is made relative to a set of threshold levels simultaneously by means of a one-to-many current mirror circuit. In improved write or erase circuits, verification of the written or erased data is done in parallel on a group of memory cells at a time and a circuit selectively inhibits further write or erase to those cells which have been correctly verified. Other improvements includes programming the ground state after erase, independent and variable power supply for the control gate of EEprom memory cells.

47 Claims, 21 Drawing Sheets



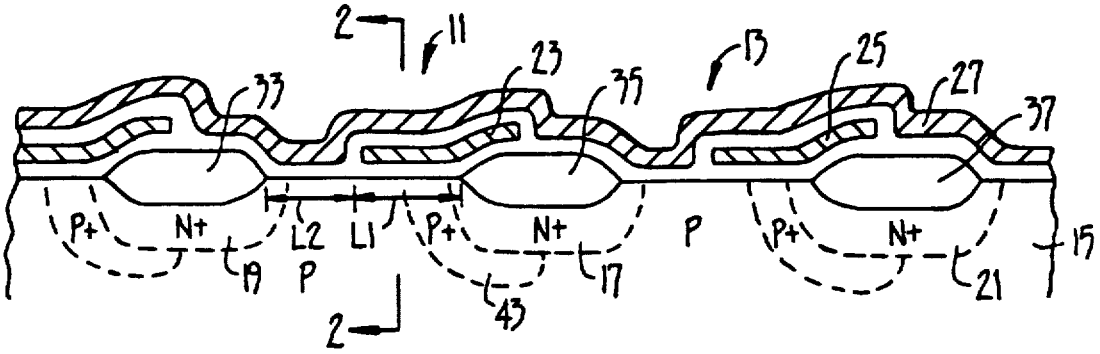


FIG._1.

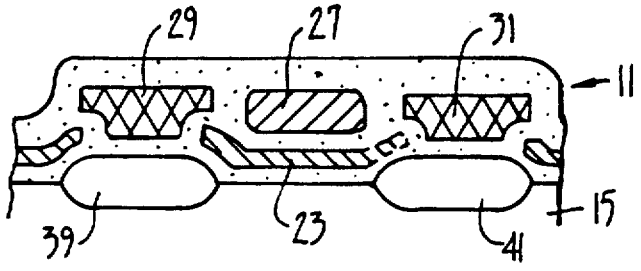


FIG._2.

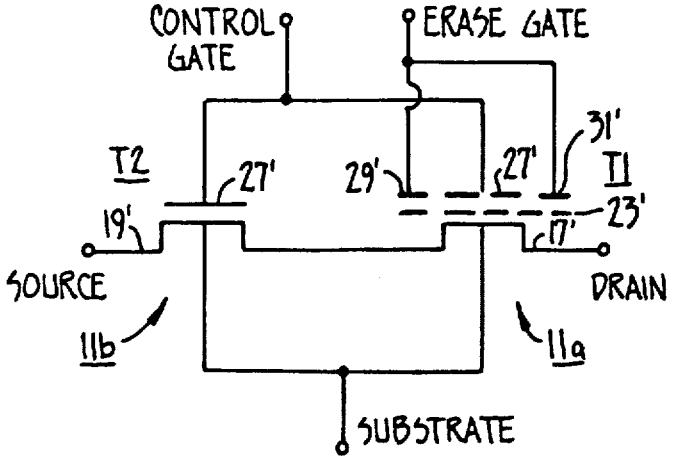


FIG._3.

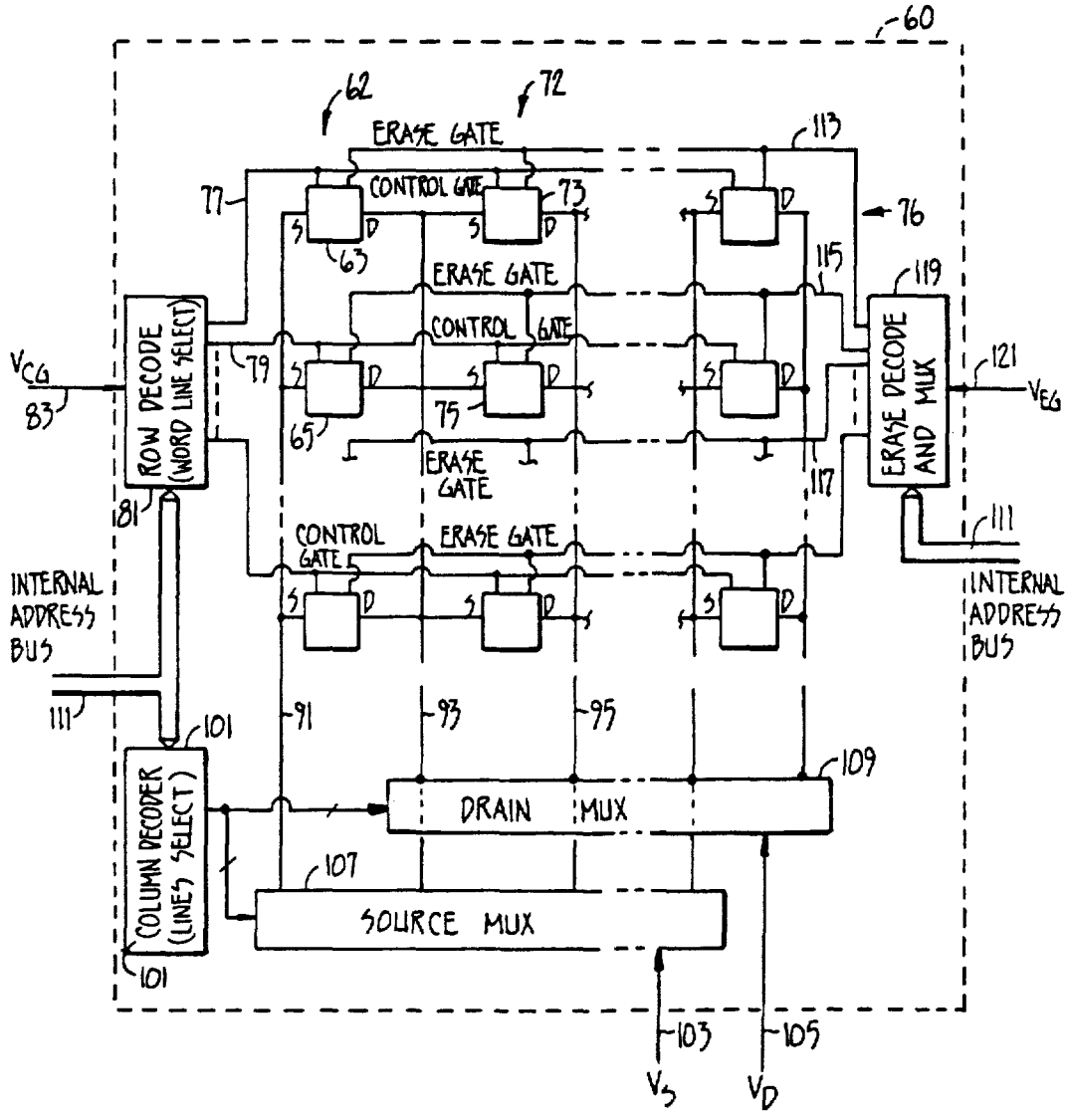

60
62
72
ERASE GATE
113
CONTROL GATE
73
77
76
63
ERASE GATE
115
119
CONTROL GATE
ROW DECODE (WORD LINE SELECT)
V_{CG}
83
79
75
65
121
V_{EG}
ERASE GATE
117
ERASE DECODE AND MUX
111
CONTROL GATE
ERASE GATE
INTERNAL ADDRESS BUS
INTERNAL ADDRESS BUS
181
111
101
91
93
95
109
DRAIN MUX
COLUMN DECODER (LINES SELECT)
107
SOURCE MUX
101
103
105
V_S
V_D

FIG._4.

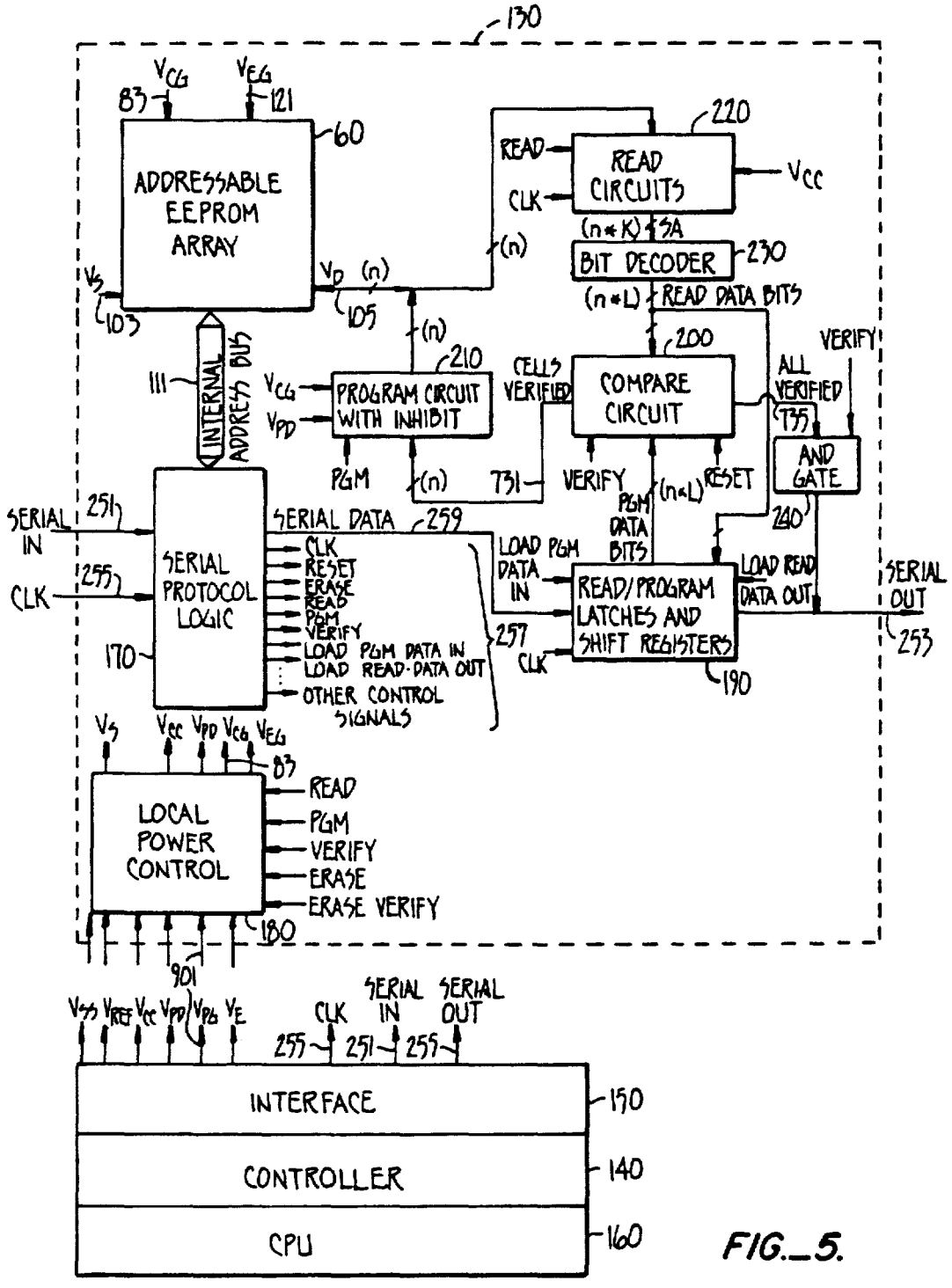

130
ADDRESSABLE EEPROM ARRAY
60
READ CIRCUITS
220
READ
CLK
Vcc
(n*K)+SA
BIT DECODER
230
(n*L) READ DATA BITS
200
COMPARE CIRCUIT
CELLS VERIFIED
ALL VERIFIED
VERIFY
T35
AND GATE
240
PROGRAM CIRCUIT WITH INHIBIT
210
INTERNAL ADDRESS BUS
111
VCG
VPD
PGM
(n)
T31
VERIFY
(n*L)
RESET
PGM DATA BITS
SERIAL IN
251
SERIAL PROTOCOL LOGIC
170
SERIAL DATA
259
CLK
RESET
ERASE
READ
PGM
VERIFY
LOAD PGM DATA IN
LOAD READ-DATA OUT
OTHER CONTROL SIGNALS
LOAD PGM DATA IN
LOAD READ DATA OUT
SERIAL OUT
253
257
CLK
READ/PROGRAM LATCHES AND SHIFT REGISTERS
190
LOCAL POWER CONTROL
83
READ
PGM
VERIFY
ERASE
ERASE VERIFY
180
901
VSS VREF VCC VPD VPB VE
CLK
SERIAL IN
SERIAL OUT
255
251
259
INTERFACE
150
CONTROLLER
140
CPU
160

FIG._5.

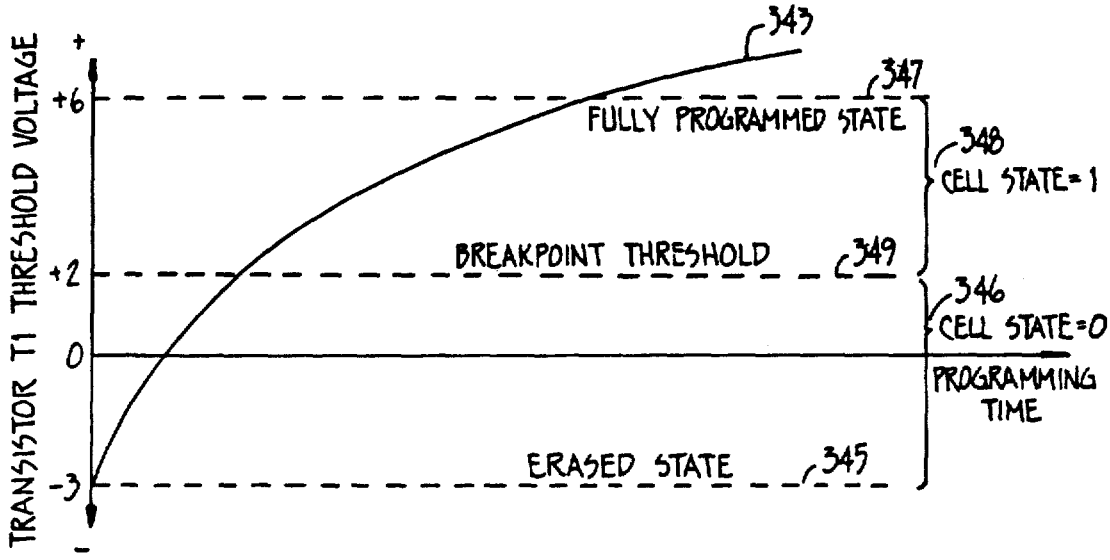

TRANSISTOR T1 THRESHOLD VOLTAGE
+
+6
+2
0
-3
-
343
347
FULLY PROGRAMMED STATE
348
CELL STATE=1
BREAKPOINT THRESHOLD
349
346
CELL STATE=0
PROGRAMMING TIME
ERASED STATE
345

FIG._6.

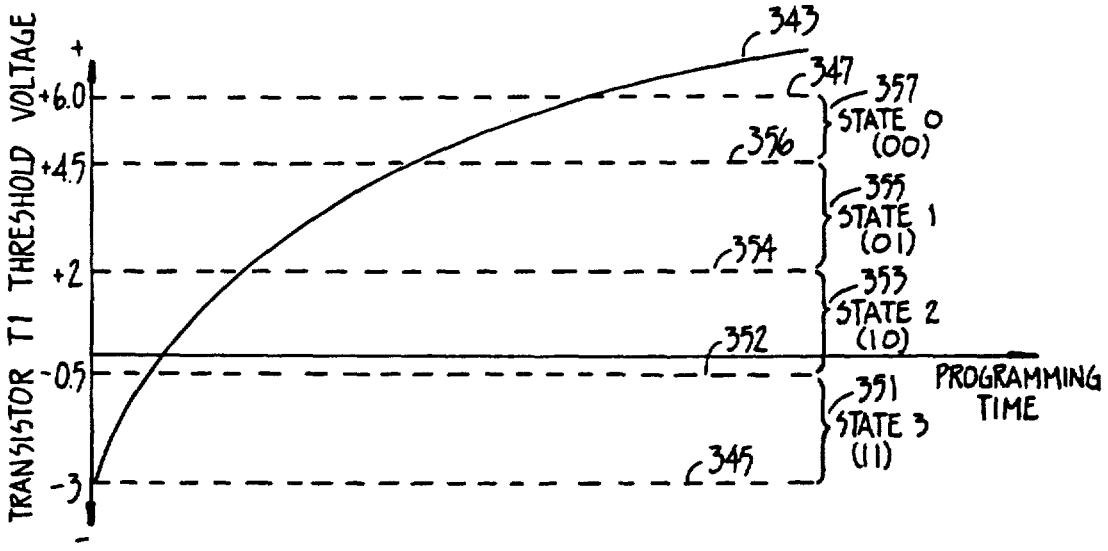

TRANSISTOR T1 THRESHOLD VOLTAGE
+
+6.0
+4.5
+2
-0.5
-3
-
343
347
357
STATE 0
(00)
356
355
STATE 1
(01)
354
353
STATE 2
(10)
352
PROGRAMMING TIME
351
STATE 3
(11)
345

FIG._7A.

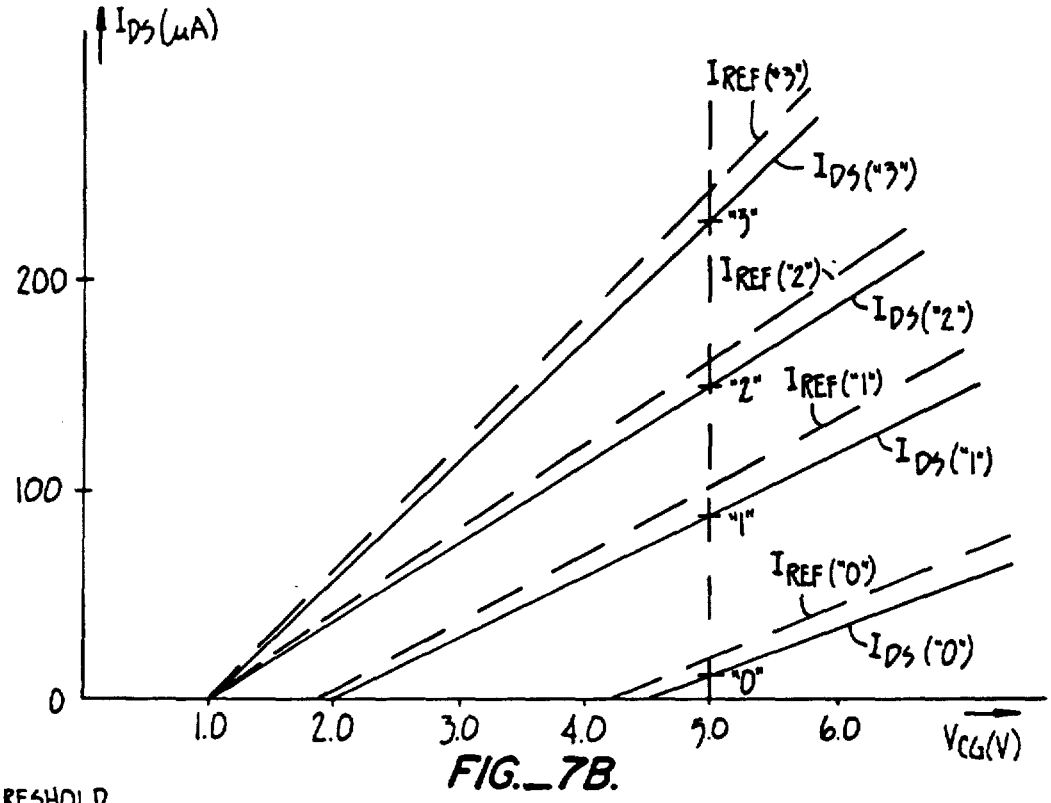


FIG._7B.

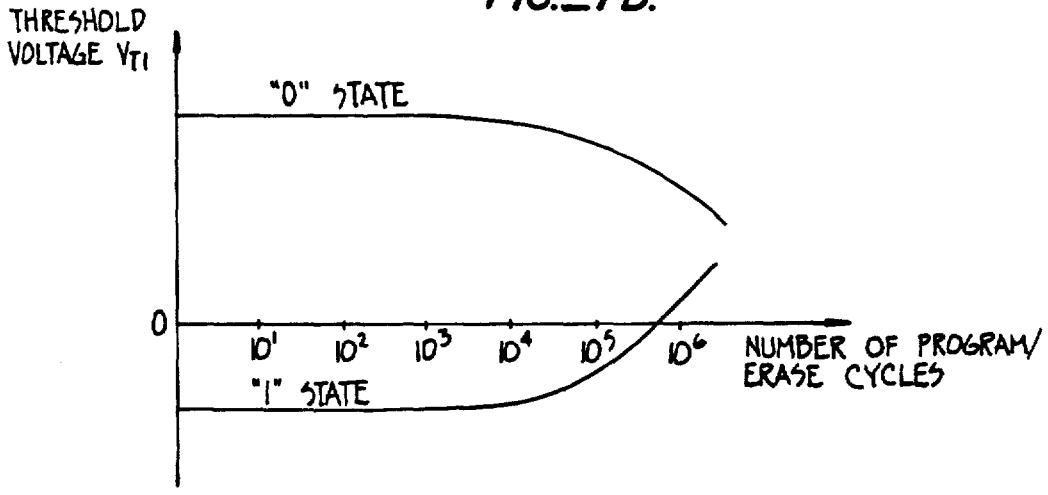


FIG._8A.

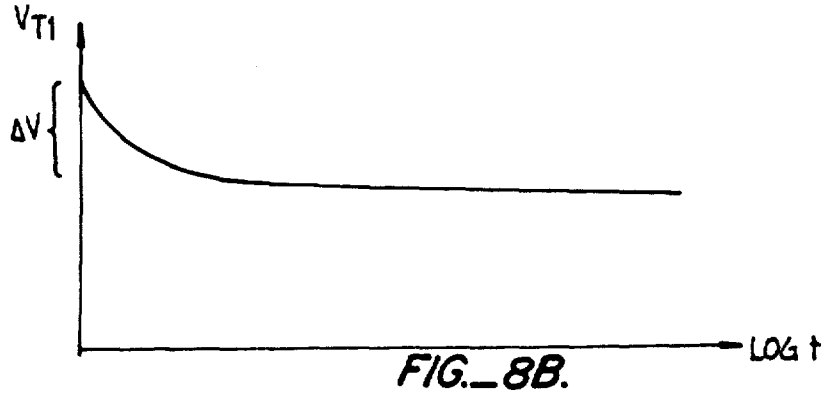


FIG._8B.

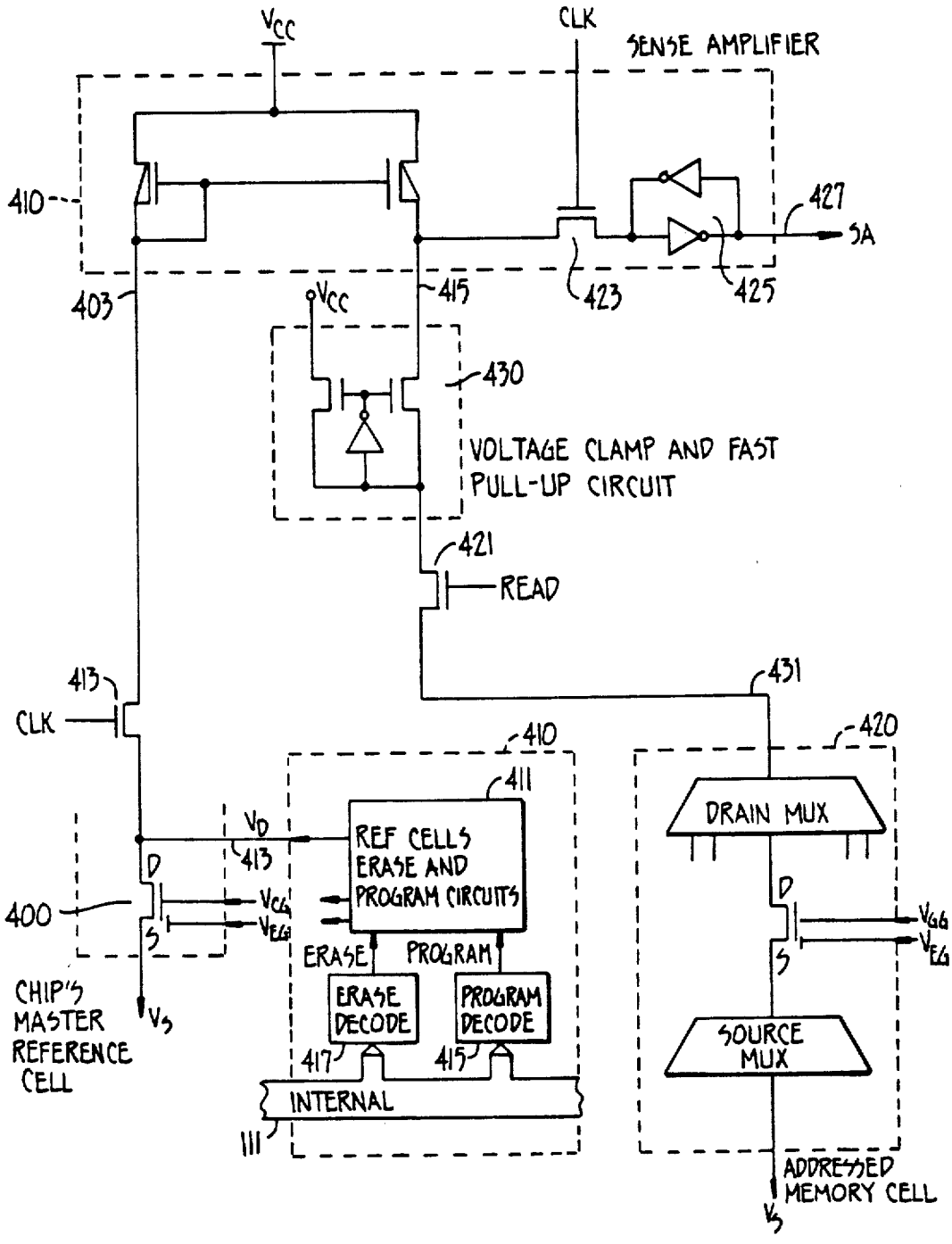

V_{CC}
CLK
SENSE AMPLIFIER
410
427
SA
403
415
423
425
V_{CC}
430
VOLTAGE CLAMP AND FAST PULL-UP CIRCUIT
421
READ
413
CLK
431
410
420
411
V_D
413
REF CELLS ERASE AND PROGRAM CIRCUITS
DRAIN MUX
D
400
V_{CG}
V_{EG}
S
ERASE
PROGRAM
V_{GG}
V_{EG}
CHIP'S MASTER REFERENCE CELL
V_S
ERASE DECODE
PROGRAM DECODE
SOURCE MUX
417
415
INTERNAL
111
ADDRESSED MEMORY CELL
V_S

FIG._9A.

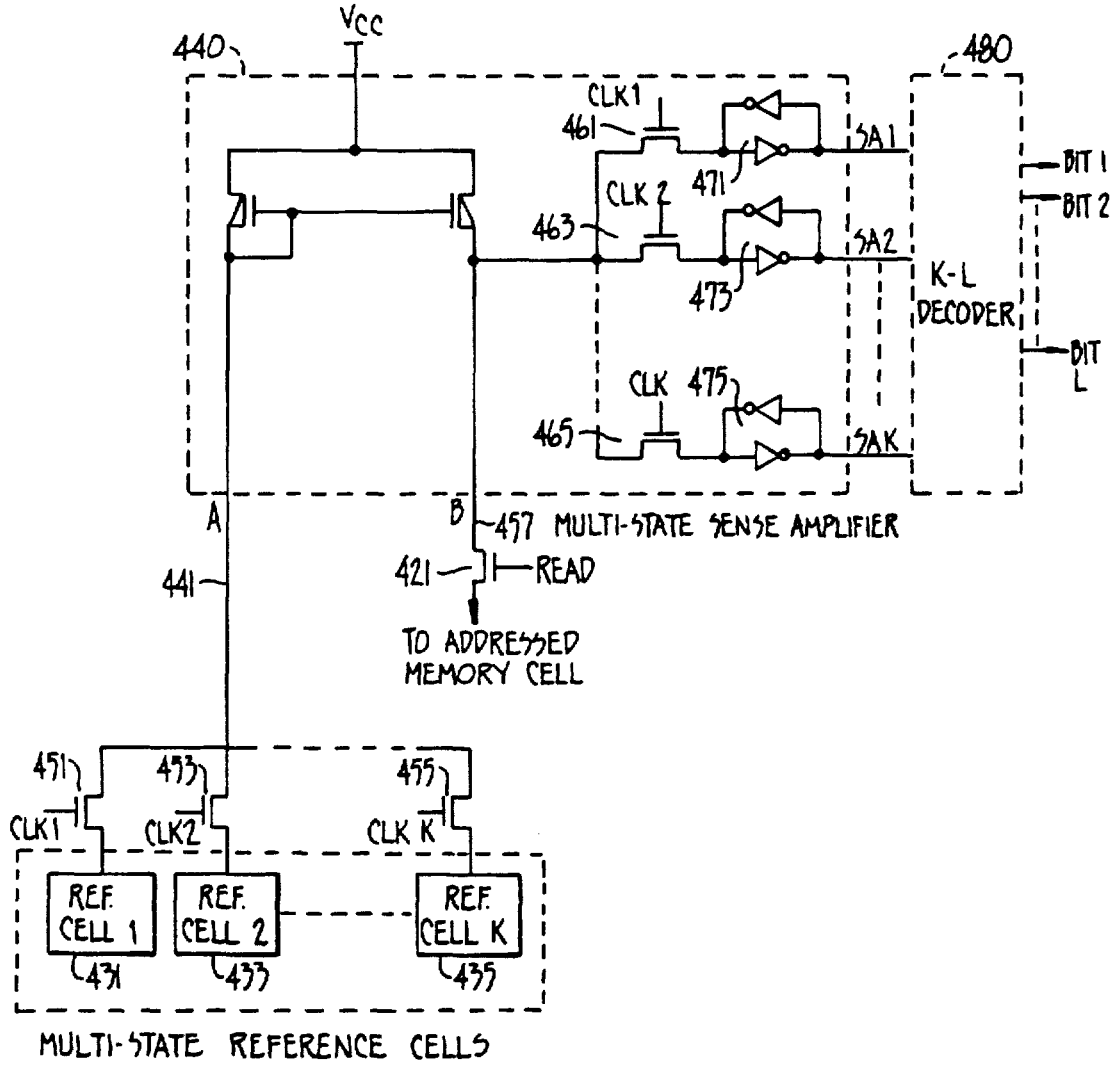

Vcc
440
480
CLK1
461
471
SA1
BIT 1
BIT 2
CLK 2
463
473
SA2
K-L
DECODER
CLK 475
465
SAK
BIT
L
A
B
457 MULTI-STATE SENSE AMPLIFIER
441
421
READ
TO ADDRESSED
MEMORY CELL
451
453
455
CLK1
CLK2
CLK K
REF.
CELL 1
REF.
CELL 2
REF.
CELL K
431
433
435
MULTI-STATE REFERENCE CELLS

FIG_9B.

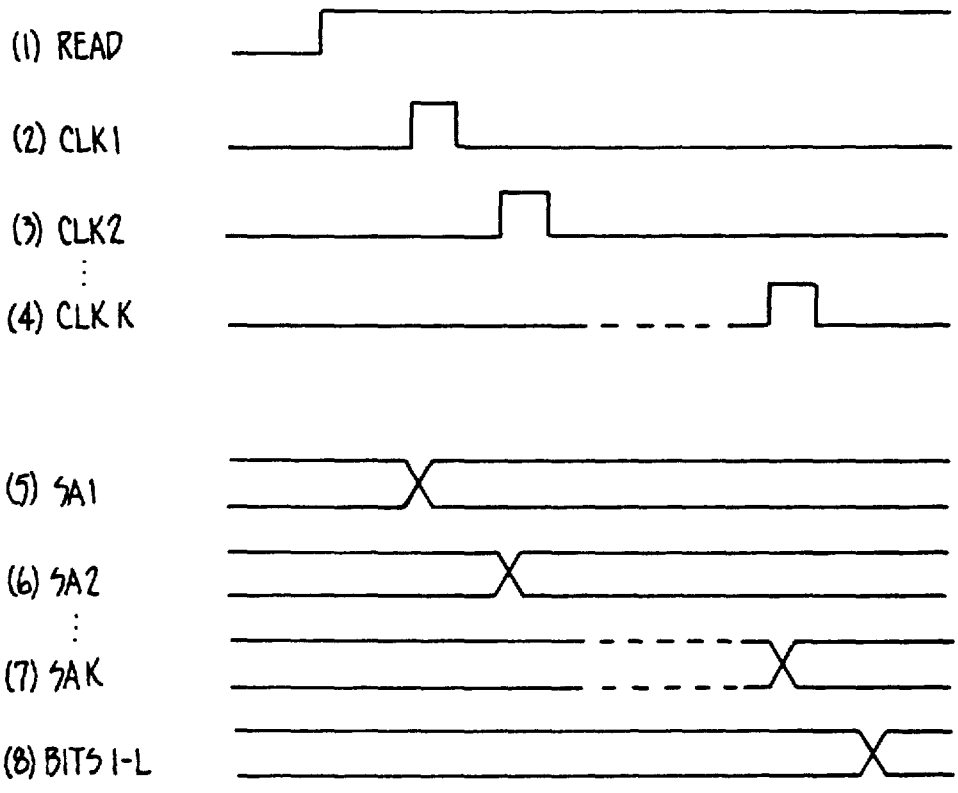

(1) READ
(2) CLK1
(3) CLK2
(4) CLK K
(5) SA1
(6) SA2
(7) SAK
(8) BITS 1-L

FIG._9C.

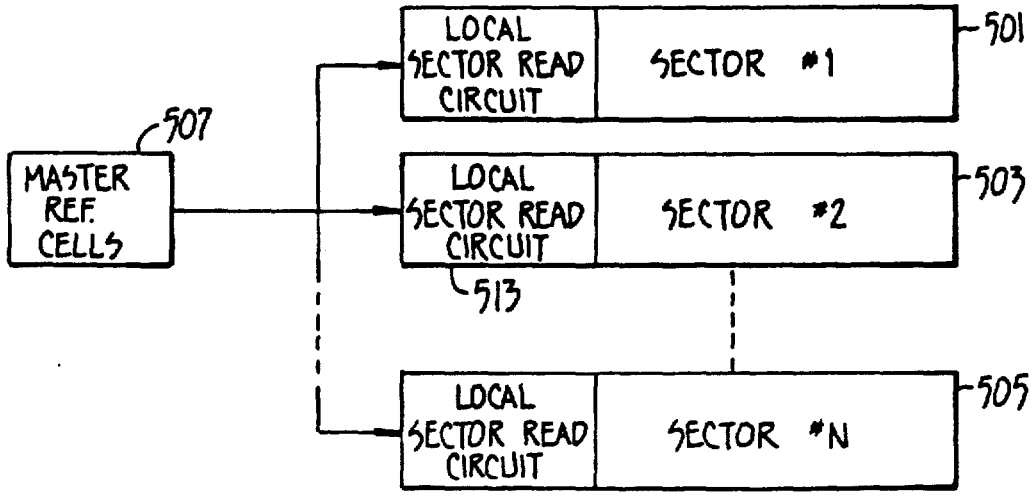

LOCAL SECTOR READ CIRCUIT
SECTOR #1
501
507
MASTER REF. CELLS
LOCAL SECTOR READ CIRCUIT
SECTOR #2
503
513
LOCAL SECTOR READ CIRCUIT
SECTOR #N
505

FIG._10.

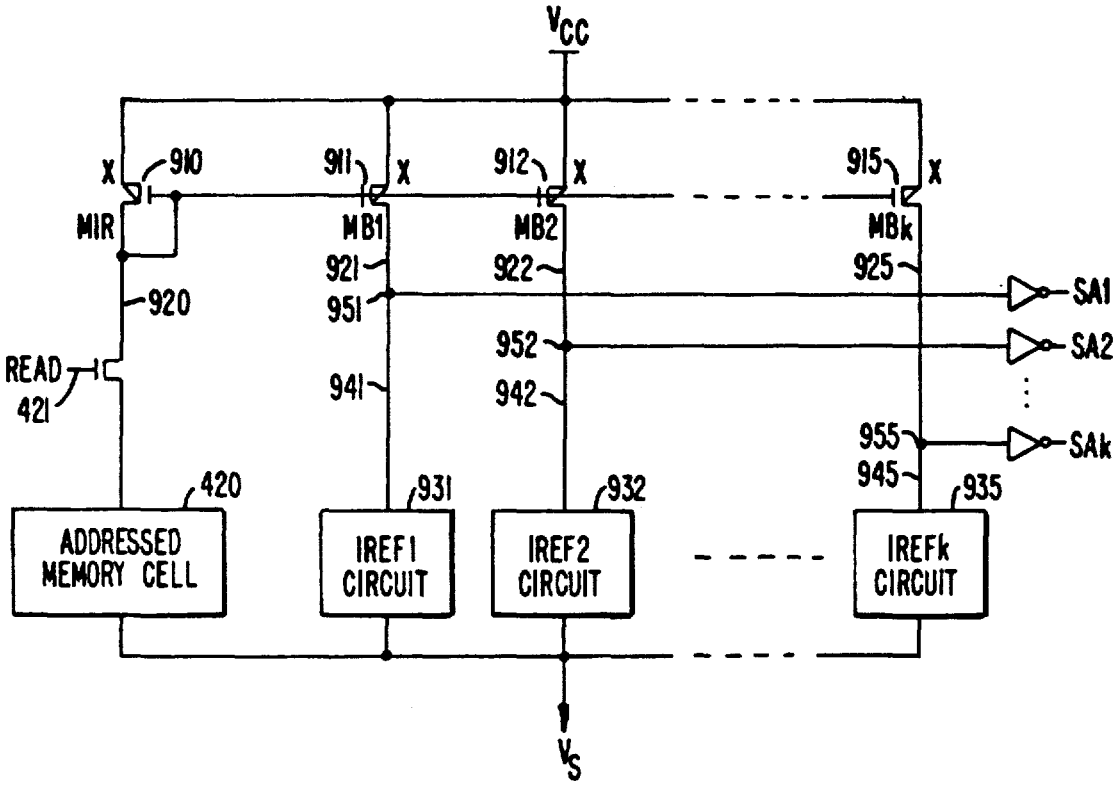

V_{CC}
X
910
911
X
912
X
915
X
MIR
MB1
MB2
MBk
921
922
925
920
951
SA1
952
SA2
READ
421
941
942
955
SAk
945
420
931
932
935
ADDRESSED MEMORY CELL
IREF1 CIRCUIT
IREF2 CIRCUIT
IREFk CIRCUIT
V_S

FIG._9D.

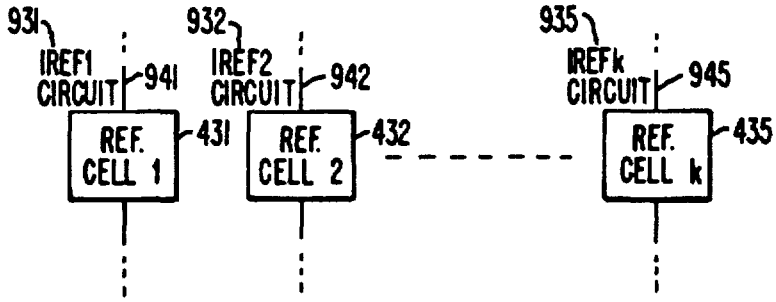

931
IREF1 CIRCUIT
941
REF. CELL 1
431
932
IREF2 CIRCUIT
942
REF. CELL 2
432
935
IREFk CIRCUIT
945
REF. CELL k
435

FIG._9E.

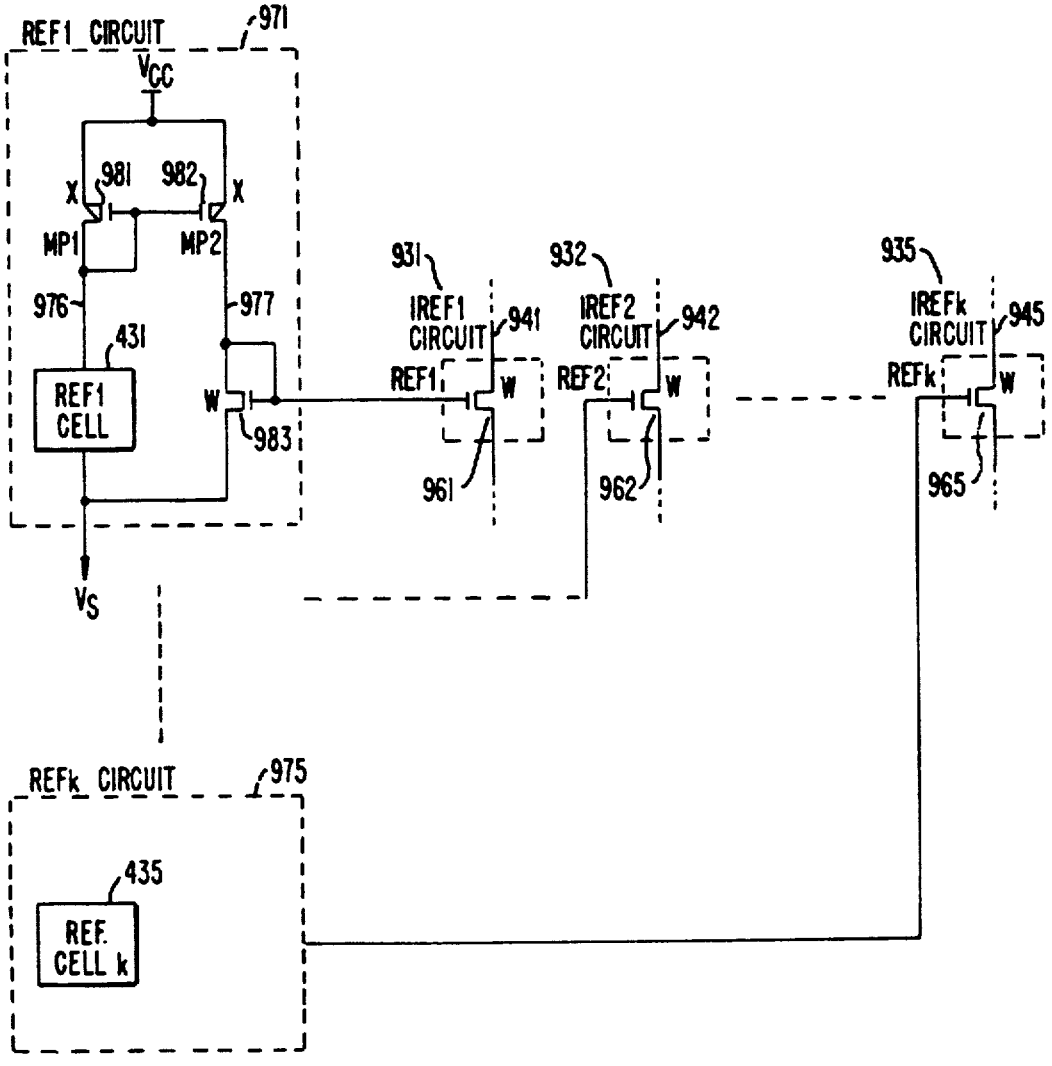

REF1 CIRCUIT
971
V_{CC}
X
981
982
X
MP1
MP2
976
977
431
REF1 CELL
W
983
V_S
931
IREF1 CIRCUIT
941
REF1
W
961
932
IREF2 CIRCUIT
942
REF2
W
962
935
IREFk CIRCUIT
945
REFk
W
965
REFk CIRCUIT
975
435
REF. CELL k

FIG._9F.

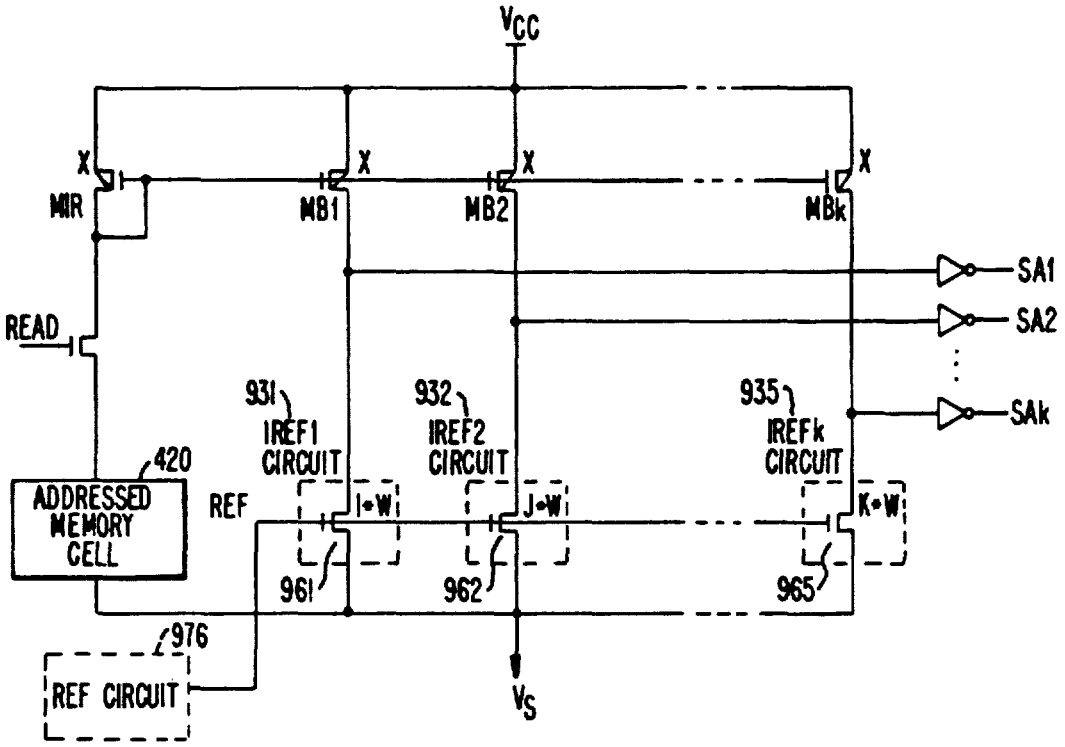

VCC
X
MIR
MB1
MB2
MBk
READ
SA1
SA2
SAk
931
IREF1 CIRCUIT
932
IREF2 CIRCUIT
935
IREFk CIRCUIT
420
ADDRESSED MEMORY CELL
REF
I*W
J*W
K*W
961
962
965
976
REF CIRCUIT
VS

FIG._9G.

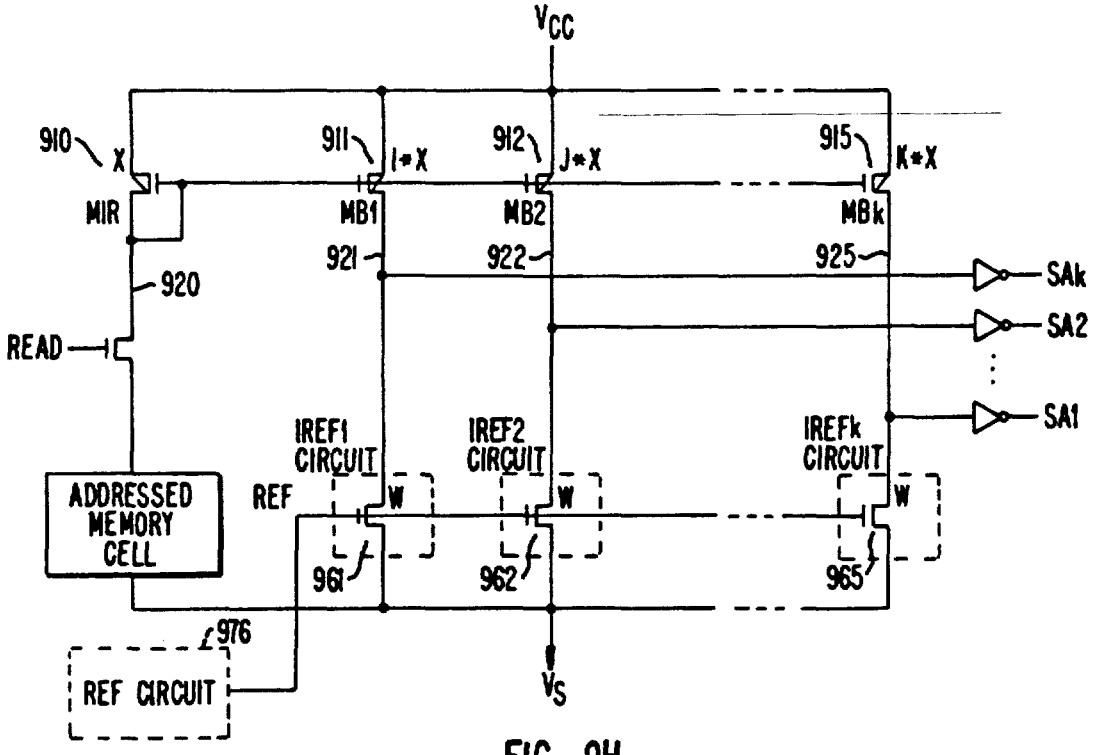

VCC
910
X
911
I*X
912
J*X
915
K*X
MIR
MB1
MB2
MBk
920
921
922
925
SAk
SA2
SA1
READ
IREF1 CIRCUIT
IREF2 CIRCUIT
IREFk CIRCUIT
ADDRESSED MEMORY CELL
REF
W
961
962
965
976
REF CIRCUIT
VS

FIG._9H.

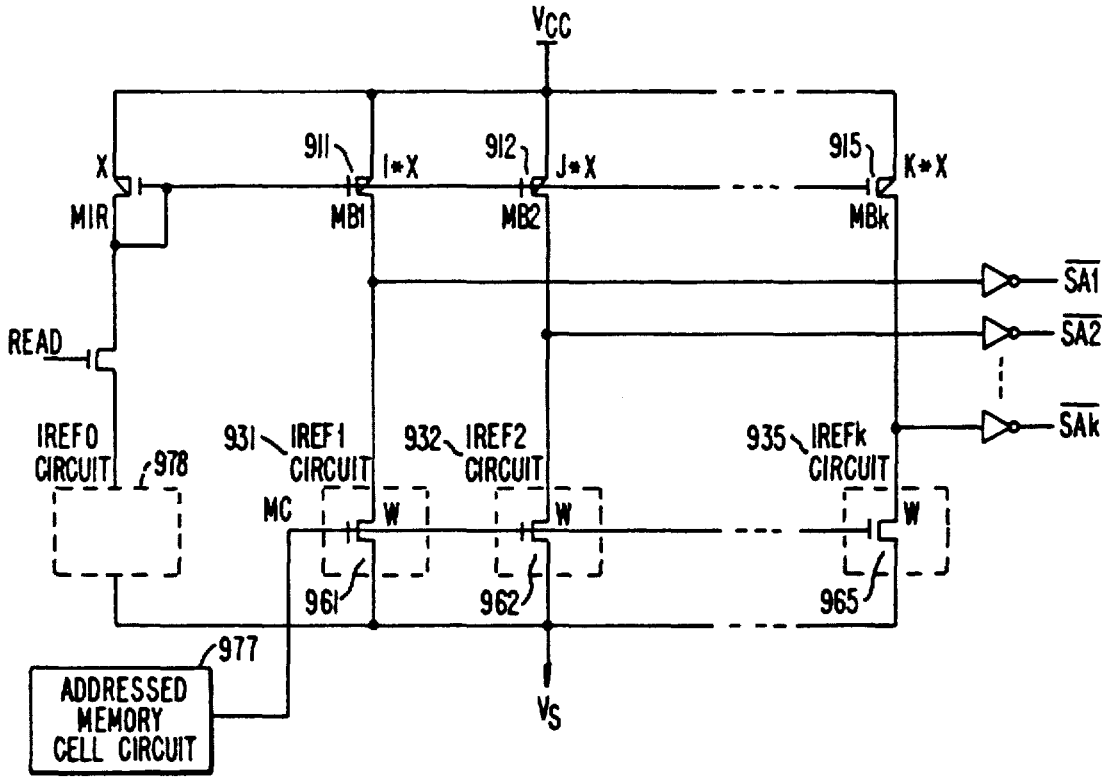

VCC
X
MIR
911
I*X
MB1
912
J*X
MB2
915
K*X
MBk
READ
SA1
SA2
SAk
IREF0 CIRCUIT
978
931
IREF1 CIRCUIT
932
IREF2 CIRCUIT
935
IREFk CIRCUIT
MC
W
961
962
965
977
ADDRESSED MEMORY CELL CIRCUIT
VS

FIG._9I.

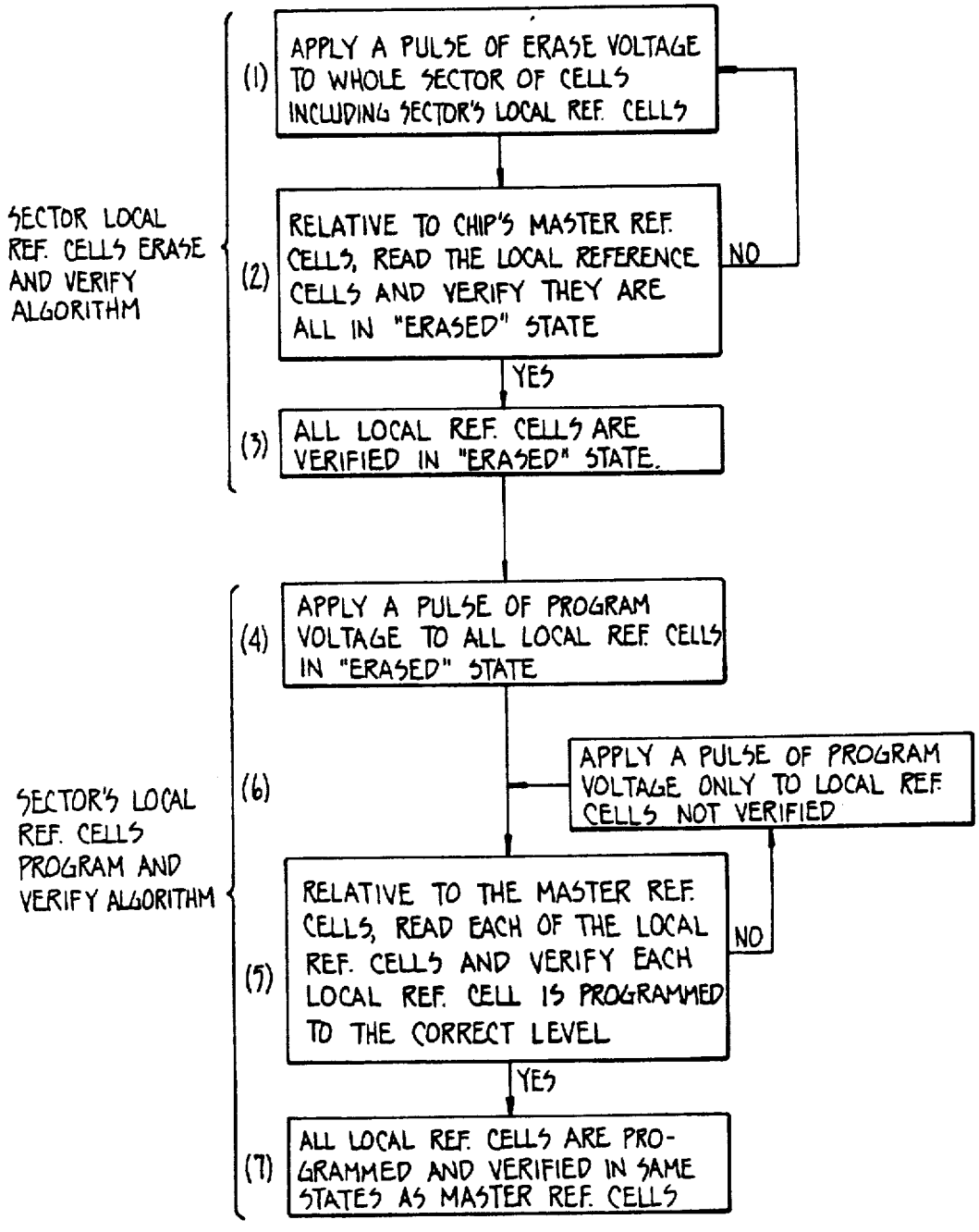

SECTOR LOCAL REF. CELLS ERASE AND VERIFY ALGORITHM
(1) APPLY A PULSE OF ERASE VOLTAGE TO WHOLE SECTOR OF CELLS INCLUDING SECTOR'S LOCAL REF. CELLS
(2) RELATIVE TO CHIP'S MASTER REF. CELLS, READ THE LOCAL REFERENCE CELLS AND VERIFY THEY ARE ALL IN "ERASED" STATE
NO
YES
(3) ALL LOCAL REF. CELLS ARE VERIFIED IN "ERASED" STATE.
SECTOR'S LOCAL REF. CELLS PROGRAM AND VERIFY ALGORITHM
(4) APPLY A PULSE OF PROGRAM VOLTAGE TO ALL LOCAL REF. CELLS IN "ERASED" STATE
(6) APPLY A PULSE OF PROGRAM VOLTAGE ONLY TO LOCAL REF. CELLS NOT VERIFIED
(5) RELATIVE TO THE MASTER REF. CELLS, READ EACH OF THE LOCAL REF. CELLS AND VERIFY EACH LOCAL REF. CELL IS PROGRAMMED TO THE CORRECT LEVEL
NO
YES
(7) ALL LOCAL REF. CELLS ARE PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CELLS

FIG. 11.

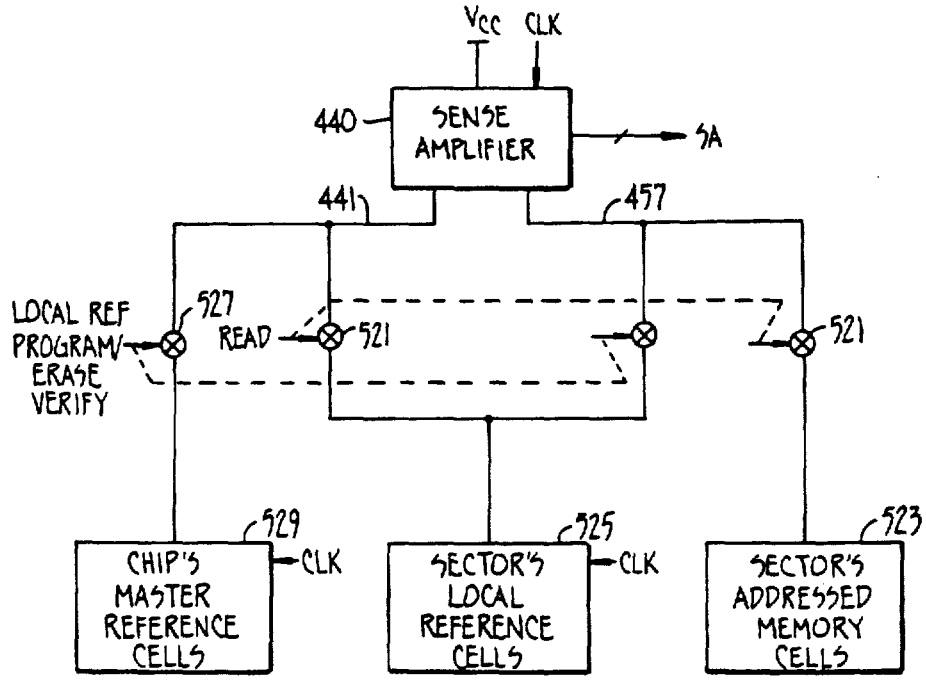


FIG._12A.

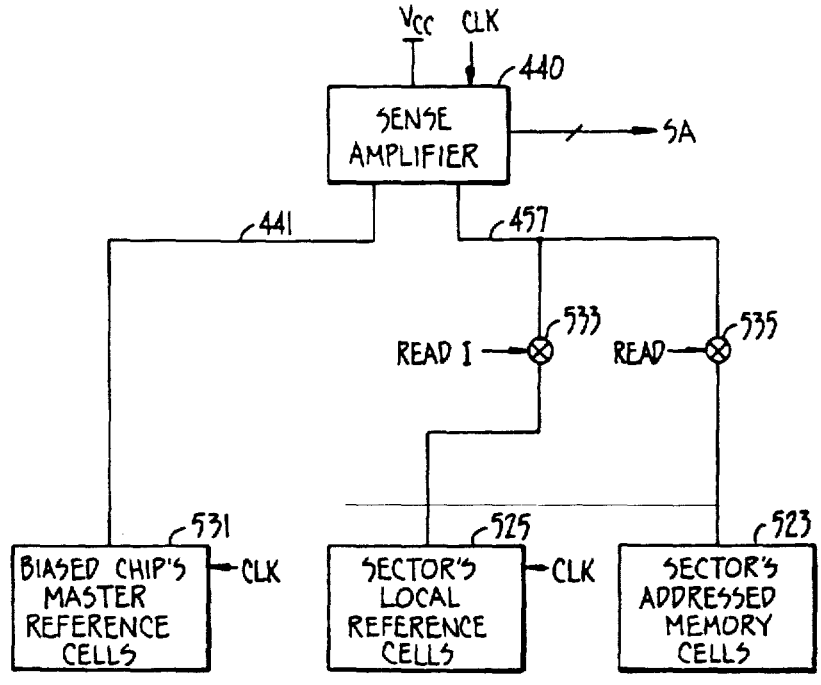


FIG._13A.

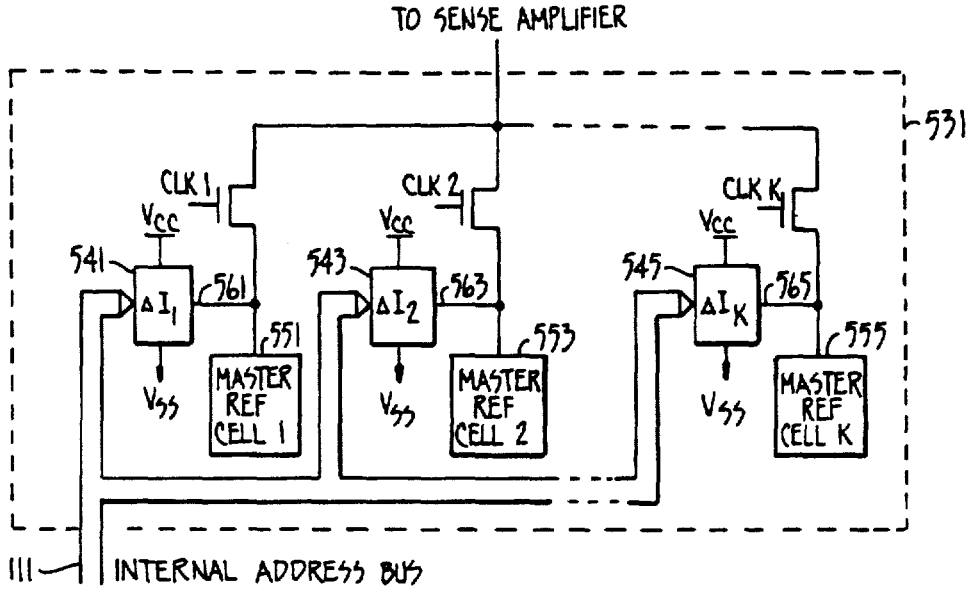


FIG._13B.

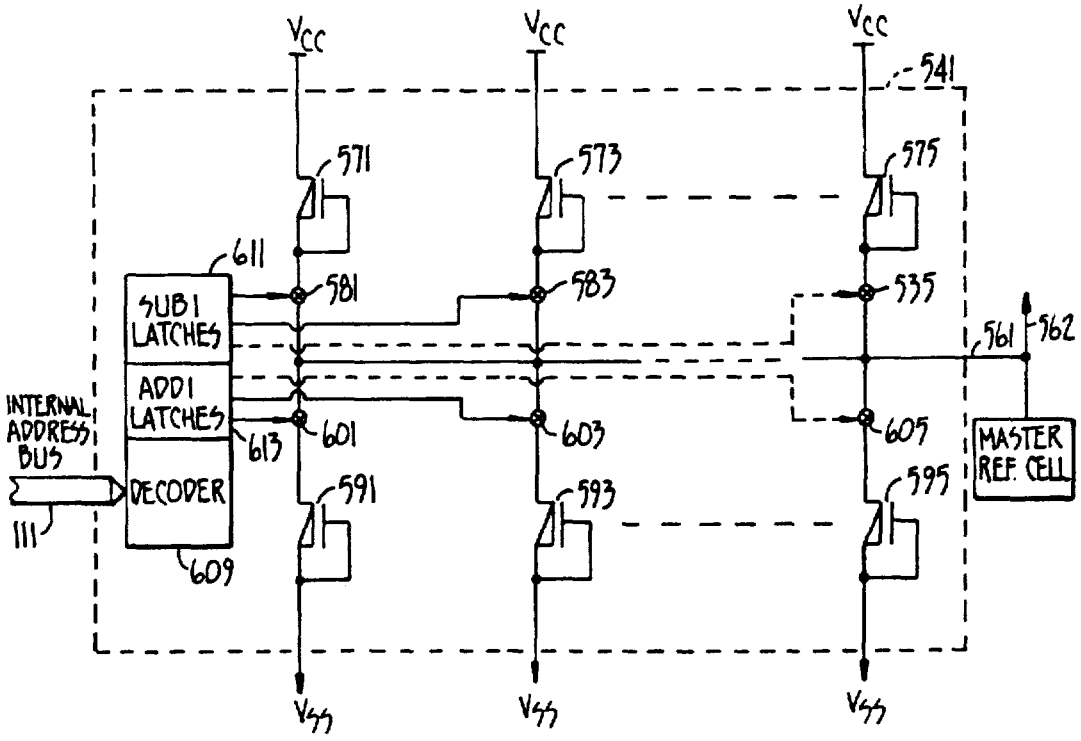


FIG._13C.

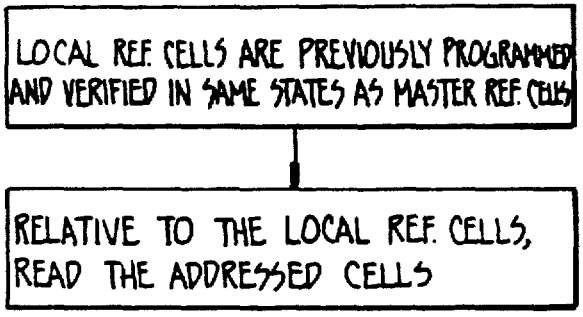


FIG._12B.

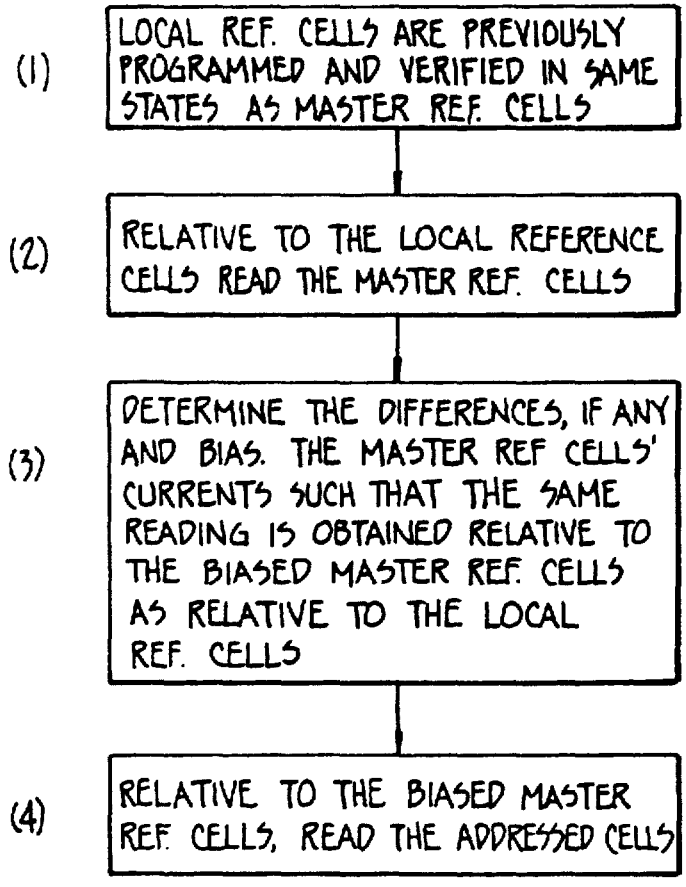
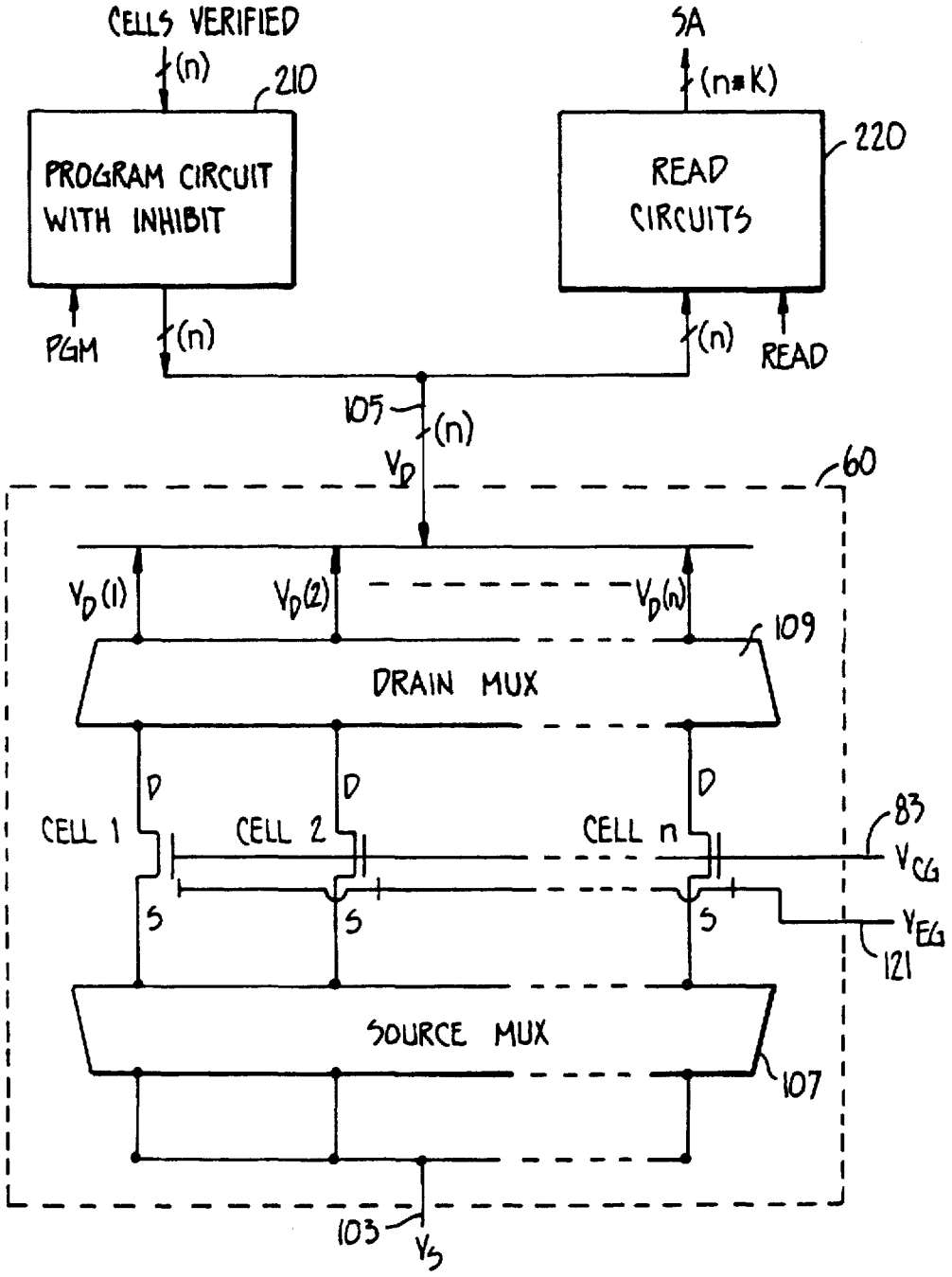
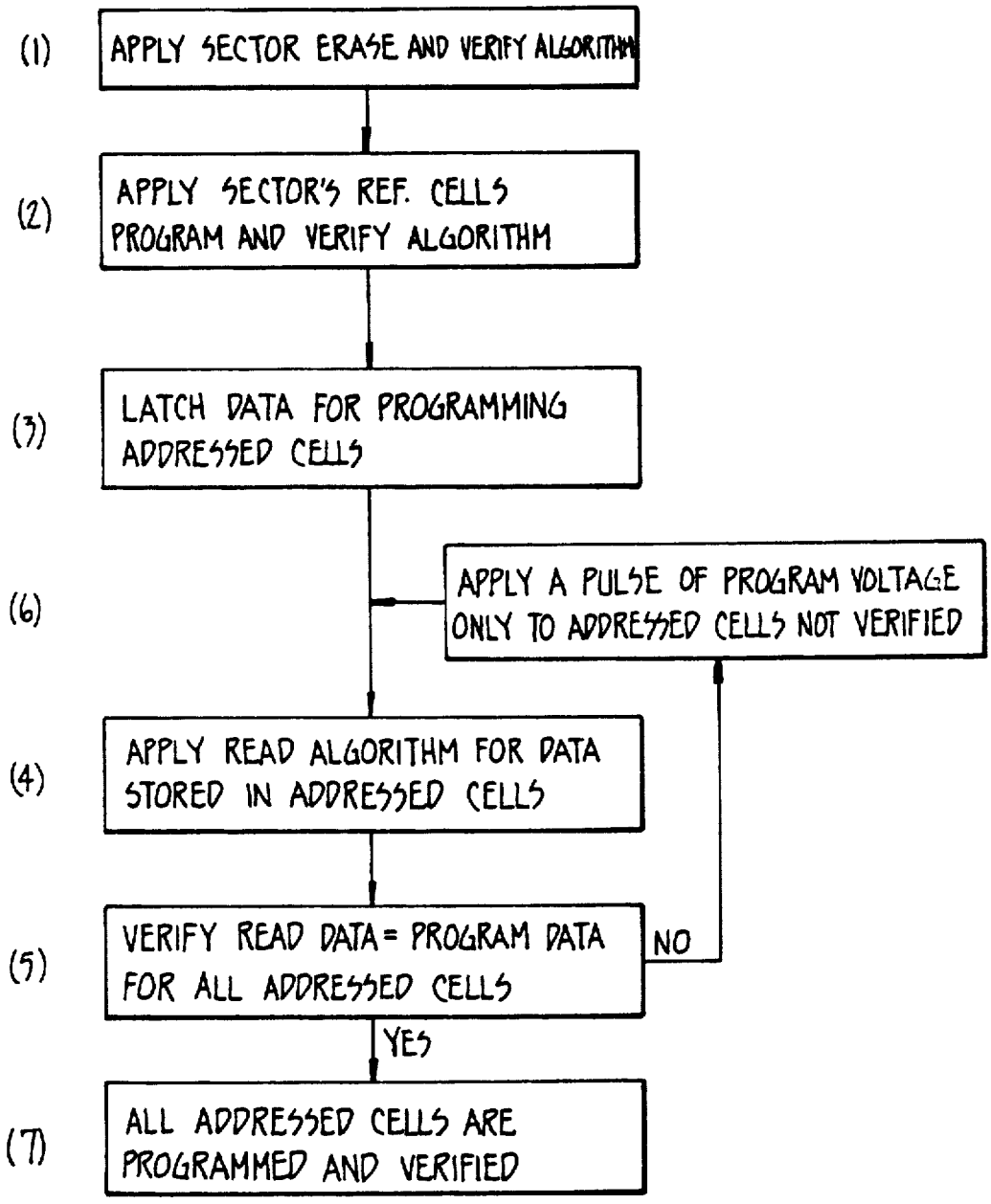


FIG._13D.



READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG_14.



PROGRAM ALGORITHM

FIG._15.

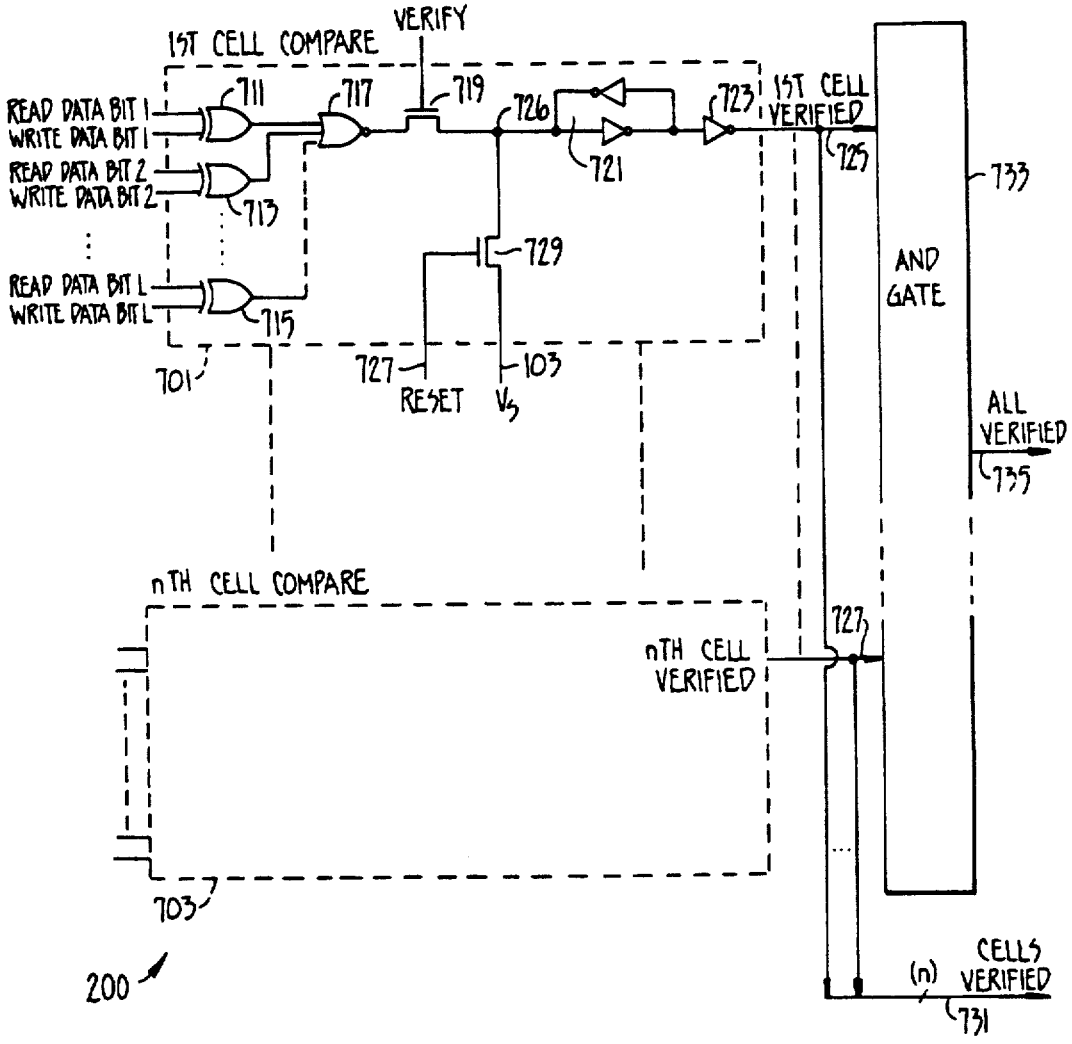

1ST CELL COMPARE
VERIFY
READ DATA BIT 1
WRITE DATA BIT 1
READ DATA BIT 2
WRITE DATA BIT 2
READ DATA BIT L
WRITE DATA BIT L
711
717
719
726
723
721
713
715
729
727
RESET
103
701
1ST CELL VERIFIED
725
733
AND GATE
ALL VERIFIED
735
nTH CELL COMPARE
nTH CELL VERIFIED
727
703
200
CELLS VERIFIED
(n)
731

FIG._16.

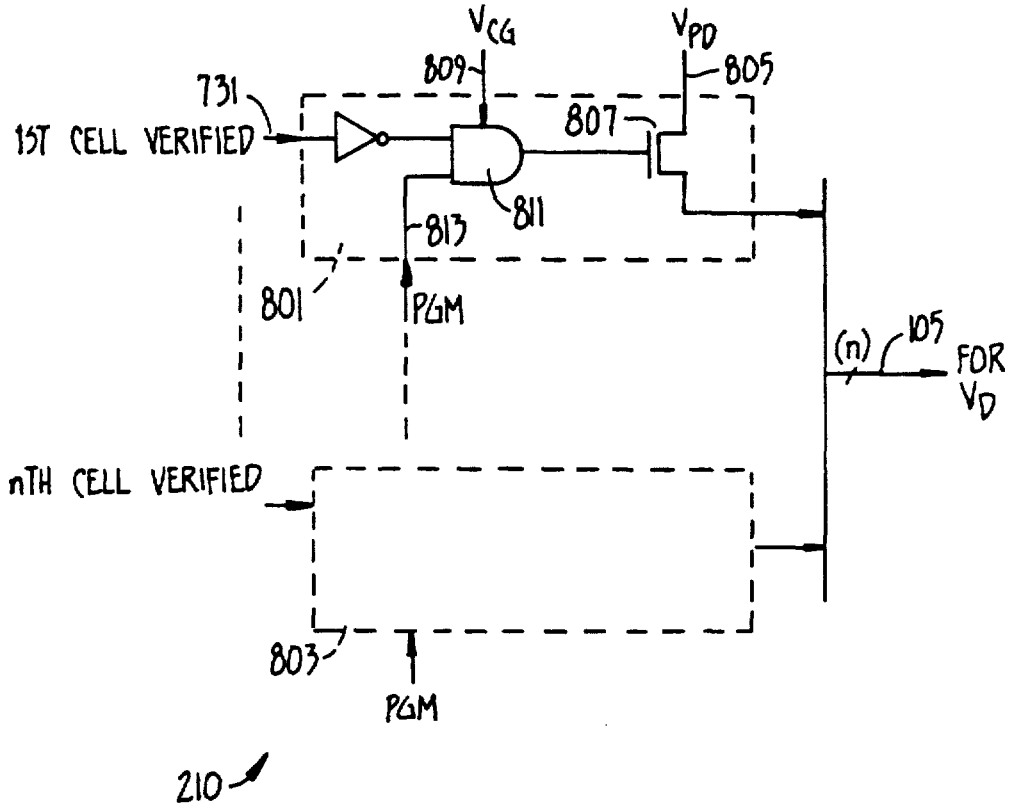

V_{CG}
V_{PD}
809
805
731
1ST CELL VERIFIED
807
811
813
801
PGM
(n)
105
FOR V_D
nTH CELL VERIFIED
803
PGM
210

FIG_17.

	SELECTED CONTROL GATE V_{CG}	DRAIN V_D	SOURCE V_S	ERASE GATE V_{EG}
READ	V_{PG}	V_{REF}	V_{SS}	V_E
PROGRAM	V_{PG}	V_{PD}	V_{SS}	V_E
PROGRAM VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E

FIG. 18.

(TYPICAL VALUES)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V_{PG}	V_{CC}	12V	$V_{CC}+\delta V$	V_{CC}	$V_{CC}-\delta V$
V_{CC}	5V	5V	5V	5V	5V
V_{PD}	V_{SS}	8V	8V	V_{SS}	V_{SS}
V_E	V_{SS}	V_{SS}	V_{SS}	20V	V_{SS}
UNSELECTED CONTROL GATE	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
UNSELECTED BIT LINE	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}

$V_{SS}=0V$, $V_{REF}=1.5V$, $\delta V=0.5V-1V$

FIG. 19.

MULTI-STATE EEPROM READ AND WRITE CIRCUITS AND TECHNIQUES

BACKGROUND OF THE INVENTION

This application is a continuation-in-part of application Ser. No. 337,579 filed Apr. 13, 1989.

This invention relates generally to semiconductor electrically erasable programmable read only memories (EEprom), and specifically to circuits and techniques for reading and programming their state.

EEprom and electrically programmable read only memory (Eprom) are typically used in digital circuits for non-volatile storage of data or program. They can be erased and have new data written or "programmed" into their memory cells.

An Eprom utilizes a floating (unconnected) conductive gate, in a field effect transistor structure, positioned over but insulated from a channel region in a semiconductor substrate, between source and drain regions. A control gate is then provided over the floating gate, but also insulated therefrom. The threshold voltage characteristic of the transistor is controlled by the amount of charge that is retained on the floating gate. That is, the minimum amount of voltage (threshold) that must be applied to the control gate before the transistor is turned "on" to permit conduction between its source and drain regions is controlled by the level of charge on the floating gate.

The floating gate can hold a range of charge and therefore an Eprom memory cell can be programmed to any threshold level within a threshold window. The size of the threshold window, delimited by the minimum and maximum threshold levels of the device, depends on the device's characteristics, operating conditions and history. Each distinct threshold level within the window may, in principle, be used to designate a definite memory state of the cell.

For Eprom memory, the transistor serving as a memory cell is programmed to one of two states by accelerating electrons from the substrate channel region, through a thin gate dielectric and onto the floating gate. The memory states are erasable by removing the charge on the floating gate by ultra-violet radiation.

An electrically erasable and programmable read only memory (EEprom) has a similar structure but additionally provides a mechanism for removing charge from its floating gate upon application of proper voltages. An array of such EEprom cells is referred to as a "Flash" EEprom array when an entire array of cells, or significant group of cells of the array, is erased simultaneously (i.e., in a flash). Once erased, a cell can then be reprogrammed.

A specific, single cell in a two-dimensional array of Eprom, EEprom cells is addressed for reading by application of a source-drain voltage to source and drain lines in a column containing the cell being addressed, and application of a control gate voltage to a word line connected to the control gates in a row containing the cell being addressed.

An addressed memory cell transistor's state is read by placing an operating voltage across its source and drain and on its control gate, and then detecting the level of current flowing between the source and drain. The level of current is proportional to the threshold level of the transistor, which in turn is determined by the amount of charge on its floating gate.

In the usual two-state EEprom cell, one breakpoint threshold level is established so as to partition the threshold window into two regions. The source/drain current is compared with the breakpoint threshold level that was used when the cell was programmed. If the current read is higher than that of the threshold, the cell is determined to be in a "zero" state, while if the current is less than that of the threshold, the cell is determined to be in the other state. Thus, such a two-state cell stores one bit of digital information. A current source which may be externally programmable is often provided as part of a memory system to generate the breakpoint threshold current.

Thus, for a multi-state EEprom memory cell, each cell stores two or more bits of data. The information that a given EEprom array can store is thus increased by the multiple of number of states that each cell can store.

Accordingly, it is a primary object of the present invention to provide a system of EEprom memory cells wherein the cells are utilized to store more than one bit of data.

It is a further object of the present invention to provide improved read circuits as part of an Eprom or EEprom integrated circuit memory chip.

It is also an object of the invention to provide read circuits which are simpler, easier to manufacture and have improved accuracy and reliability over an extended period of use.

It is also an object of the present invention to provide improved program circuits as part of an Eprom or EEprom integrated circuit memory chip.

It is also an object of the invention to provide program circuits which are simpler, easier to manufacture and have improved accuracy and reliability over an extended period of use.

It is another object of the present invention to provide memory read and program techniques that automatically compensate for effects of temperature, voltage and process variations, and charge retention.

It is yet another object of the present invention to provide Flash EEprom semiconductor chips that can replace magnetic disk storage devices in computer systems.

Further, it is an object of the present invention to provide a Flash EEprom structure capable of an increased lifetime as measured by the number of program/read cycles that the memory can endure.

SUMMARY OF THE INVENTION

These and additional objects are accomplished by improvements in EEprom array read and write circuits and techniques in order to provide multiple threshold levels that allow accurate reading and writing of more than two distinct states within each memory cell over an extended lifetime of the memory cells, so that more than one bit may be reliably stored in each cell.

According to one aspect of the present invention, the multiple threshold breakpoint levels are provided by a set of memory cells which serves as master reference cells. The master reference cells are independently and externally programmable, either by the memory manufacturer or the user. This feature provides maximum flexibility, allowing the breakpoint thresholds to be individually set within the threshold window of the device at any time. Also, by virtue of being an identical device as that of the memory cells, the reference cells closely track the same variations due to manufacturing

processes, operating conditions and device aging. The independent programmability of each breakpoint threshold level allows optimization and fine-tuning of the threshold window's partitioning, critical in multi-state implementation. Furthermore, it allows post-manufacture configuration for either 2-state or multi-state memory from the same device, depending on user need or device characteristics at the time.

According to another aspect of the present invention, a set of memory cells within each sector (where a sector is a group of memory cells which are all erased at the same time in a Flash EEprom) are set aside as local reference cells. Each set of reference cells tracks the Flash cells in the same sector closely as they are both cycled through the same number of program/erase cycles. Thus, the aging that occurs in the memory cells of a sector after a large number of erase/reprogram cycles is also reflected in the local reference cells. Each time the sector of flash cells is erased and reprogrammed, the set of individual breakpoint threshold levels are re-programmed to the associated local reference cells. The threshold levels read from the local reference cells then automatically adjust to changing conditions of the memory cells of the same sector. The threshold window's partitioning is thus optimally maintained. This technique is also useful for a memory that employs only a single reference cell that is used to read two state (1 bit) memory cells.

According to another aspect of the present invention, the threshold levels rewritten at each cycle to the local reference cells are obtained from a set of master cells which are not cycled along with the memory cells but rather which retain a charge that has been externally programmed (or reprogrammed). Only a single set of master memory cells is needed for an entire memory integrated circuit.

In one embodiment, the read operation directly uses the threshold levels in the local reference cells previously copied from the master reference cells. In another embodiment, the read operation indirectly uses the threshold levels in the local reference cells even though the reading is done relative to the master reference cells. It does this by first reading the local reference cells relative to the master reference cells. The differences detected are used to offset subsequent regular readings of memory cells relative to the master reference cells so that the biased readings are effectively relative to the local reference cells.

According to another aspect of the present invention, a read operation on a memory cell determines which memory state it is in by comparing the current flowing therethrough with that of a set of reference currents corresponding to the multiple threshold breakpoint levels.

In one embodiment, the current flowing through a cell being read is compared one-by-one with each of the threshold current levels of the reference cells.

In another embodiment, the current flowing through a cell to be read is compared simultaneously with that of the set of reference cells. A special current mirror configuration reproduces the current to be read without degrading its signal, into multiple branches, one for each threshold current comparison.

According to another aspect of the present invention, where a programmed state is obtained by repetitive steps of programming and verifying from the "erased" state, a circuit verifies the programmed state after each programming step with the intended state and selectively inhibits further programming of any cells in the chunk that have been verified to have been programmed correctly. This enables efficient parallel programming of a chunk of data in a multi-state implementation.

According to another aspect of the present invention, where a chunk of EEprom cells are addressed to be erased in parallel, an erased state is obtained by repetitive steps of erasing and verifying from the existing state to the "erased" state, a circuit verifies the erased state after each erasing step with the "erased" state and selectively inhibits further erasing of any cells in the chunk that have been verified to have been erased correctly. This prevents over-erasing which is stressful to the device and enables efficient parallel erasing of a group of cells.

According to another aspect of the present invention, after a group of cells have been erased to the "erased" state, the cells are re-programmed to the state adjacent the "erased" state. This ensures that each erased cell starts from a well defined state, and also allows each cell to undergo similar program/erase stress.

The subject matter herein is a further development of the EEprom array read techniques described in copending patent application Ser. No. 204,175, filed Jun. 8, 1988, by Dr. Eliyahou Harari, particularly the disclosure relating to FIG. **11***e* thereof. Application Ser. No. 204,175 is hereby expressly incorporated herein by reference, the disclosure with respect to the embodiments of FIGS. **11**, **12**, **13** and **15** being most pertinent.

Additional objects, features and advantages of the present invention will be understood from the following description of its preferred embodiments, which description should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view of an EEprom device integrated circuit structure that can be used to implement the various aspects of the present invention;

FIG. **2** is a view of the structure of FIG. **1** taken across section **2**—**2** thereof;

FIG. **3** is an equivalent circuit of a single EEprom cell of the type illustrated in FIGS. **1** and **2**;

FIG. **4** shows an addressable array of EEprom cells;

FIG. **5** is a block diagram of an EEprom system in which the various aspects of the present invention are implemented;

FIG. **6** illustrates the partitioning of the threshold window of an EEprom cell which stores one bit of data;

FIG. **7A** illustrates the partitioning of the threshold window of an EEprom cell which stores two bits of data;

FIG. **7B** illustrates the partitioning of the source-drain conduction current threshold window of the EEprom cell of FIG. **7A**;

FIGS. **8A** and **8B** are curves that illustrate the changes and characteristics of a typical EEprom after a period of use;

FIG. **9A** illustrates read and program circuits for a master reference cell and an addressed memory cell according to the present invention;

FIG. **9B** illustrates multi-state read circuits with reference cells according to the present invention;

FIGS. **9C(1)**–**9C(8)** illustrate the timing for multi-state read for the circuits of FIG. **9B**;

FIG. **9D** illustrates one embodiment of a multi-state read circuit in which the memory state of an address

cell is sensed relative to a set of reference current levels simultaneously;

FIG. 9E illustrates one embodiment of an IREF circuit shown in FIG. 9D as an EEprom cell programmed with a reference current;

FIG. 9F illustrates a preferred implementation of the embodiment in FIG. 9D in which each IREF circuit is provided by a current source reproducing a reference current programmed in the EEprom cell;

FIG. 9G illustrates another embodiment of an IREF circuit shown in FIG. 9D in which a reference current is provided in each branch by the conduction of a transistor of predetermined size;

FIG. 9H illustrates another embodiment of a multi-state read circuit in which the memory state of an address cell is sensed relative to a set of reference current levels simultaneously;

FIG. 9I illustrates yet another embodiment of a multi-state read circuit in which the memory state of an address cell is sensed relative to a set of reference current levels simultaneously;

FIG. 10 illustrates a specific memory organization according to the present invention;

FIG. 11 shows an algorithm for programming a set of local reference cells according to the present invention;

FIG. 12A shows one embodiment of a read circuit using local reference cells directly;

FIG. 12B shows a read algorithm for the embodiment of FIG. 12A;

FIG. 13A shows an alternative embodiment of a read circuit using local reference cells indirectly;

FIG. 13B is a programmable circuit for the biased reading of the master reference cells according the alternative embodiment;

FIG. 13C is a detail circuit diagram for the programmable biasing circuit of FIG. 13B;

FIG. 13D shows a read algorithm for the embodiment of FIG. 13A;

FIG. 14 illustrates the read/program data paths for a chunk of cell in parallel;

FIG. 15 shows an on chip program/verify algorithm according to the present invention;

FIG. 16 is a circuit diagram for the compare circuit according to the present invention;

FIG. 17 is a circuit diagram for the program circuit with inhibit according to the present invention;

FIGS. 18 and 19 show Tables 1 and 2 which list typical examples of operating voltages for the EEprom cell of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

There are many specific Eprom, EEprom semiconductor integrated circuit structures that can be utilized in making a memory array with which the various aspects of the present invention are advantageously implemented.

"Split-Channel" EEprom Cell

A preferred EEprom structure is generally illustrated in the integrated circuit cross-sectional views of FIGS. 1 and 2. Describing this preferred structure briefly, two memory cells 11 and 13 are formed on a lightly p-doped substrate 15. A heavily n-doped implanted region 17 between the cells 11 and 13 serves as a drain for the cell 11 and a source for the cell 13. Similarly, another implanted n-doped region 19 is the source of the cell 11 and the drain of an adjacent cell, and similarly for another n-doped region 21.

Each of the memory cells 11 and 13 contains respective conductive floating gates 23 and 25, generally made of polysilicon material. Each of these floating gates is surrounded by dielectric material so as to be insulated from each other and any other conductive elements of the structure. A control gate 27 extends across both of the cells 11 and 13 in a manner to be insulated from the floating gates and the substrate itself. As shown in FIG. 2, conductive strips 29 and 31 are additionally provided to be insulated from each other and other conductive elements of the structure, serving as erase gates. A pair of such erase gates surrounds the floating gate of each memory cell and are separated from it by an erase dielectric layer. The cells are isolated by thick field oxide regions, such as regions 33, 35, and 37, shown in the cross-section of FIG. 1, and regions 39 and 41 shown in the view of FIG. 2.

The memory cell is programmed by transferring electrons from the substrate 15 to a floating gate, such as the floating gate 25 of the memory cell 13. The charge on the floating gate 25 is increased by electrons travelling across the dielectric from a heavily p-doped region 43 and onto the floating gate. Charge is removed from the floating gate through the dielectric between it and the erase gates 29 and 31. This preferred EEprom structure, and a process for manufacturing it, are described in detail in copending patent application Ser. No. 323,779 of Jack H. Yuan and Eliyahou Harari, filed Mar. 15, 1989, which is expressly incorporated herein by reference.

The EEprom structure illustrated in FIGS. 1 and 2 is a "split-channel" type. Each cell may be viewed as a composite transistor consisting of two transistor T1 and T2 in series as shown in FIG. 3. The T1 transistor 11*a* is formed along the length L1 of the channel of the cell 11 of FIG. 1. It has a variable threshold voltage V_{T1}. In series with the T1 transistor 11*a* is the T2 transistor 11*b* that is formed in a portion of the channel L2. It has a fixed threshold voltage V_{T2} of about 1 V. Elements of the equivalent circuit of FIG. 3 are labeled with the same reference numbers as used for corresponding parts in FIGS. 1 and 2, with a prime (') added.

As can best be seen from the equivalent circuit of FIG. 3, the level of charge on the T1's floating gate 23' of an EEprom cell affects the threshold voltage V_{T1} of the T1 transistor 11*a* when operated with the control gate 27'. Thus, a number of memory states may be defined in a cell, corresponding to well defined threshold voltages programmed into the cell by appropriate amount of charges placed on the floating gate. The programming is performed by applying, over a certain period of time, appropriate voltages to the cell's control gate 27' as well as drain 17' and source 19'.

Addressable Flash EEprom Array

The various aspects of the present invention are typically applied to an array of Flash EEprom cells in an integrated circuit chip. FIG. 4 illustrates schematically an array of individually addressable EEprom cells 60. Each cell is equivalent to the one shown in FIG. 3, having a control gate, source and drain, and an erase gate. The plurality of individual memory cells are organized in rows and columns. Each cell is addressed by selectively energizing its row and column simultaneously. A column 62, for example, includes a first memory cell 63, an adjacent second memory cell 65,

and so forth. A second column **72** includes memory cells **73**, **75**, and so forth. Cells **63** and **73** are located in a row **76**, cells **65** and **71** in another, adjacent row, and so forth.

Along each row, a word line is connected to all the control gates of the cells in the row. For example, the row **76** has the word line **77** and the next row has the word line **79**. A row decoder **81** selectively connects the control gate voltage V_{CG} on an input line **83** to all the control gates along a selected word line for a row.

Along each column, all the cells have their sources connected by a source line such as **91** and all their drains by a drain line such as **93**. Since the cells along a row are connected in series by their sources and drains, the drain of one cell is also the source of the adjacent cell. Thus, the line **93** is the drain line for the column **62** as well as the source line for the column **72**. A column decoder **101** selectively connects the source voltage V_S on an input line **103** to all the sources and connects the drain voltage V_D on an input line **105** to all the drains along a selected column.

Each cell is addressed by the row and column in which it is located. For example, if the cell **75** is addressed for programming or reading, appropriate programming or reading voltages must be supplied to the cell's control gate, source and drain. An address on the internal address bus **111** is used to decode row decoder **81** for connecting V_{CG} to the word line **79** connected to the control gate of the cell **75**. The same address is used to decode column decoder **101** for connecting V_S to the source line **93** and V_D to the drain line **95**, which are respectively connected to the source and drain of the cell **75**.

One aspect of the present invention, which will be disclosed in more detail in a later section, is the implementation of programming and reading of a plurality of memory cells in parallel. In order to select a plurality of columns simultaneously, the column decoder, in turn, controls the switching of a source multiplexer **107** and a drain multiplexer **109**. In this way, the selected plurality of columns may have their source lines and drain lines made accessible for connection to V_S and V_D respectively.

Access to the erase gate of each cell is similar to that of the control gate. In one implementation, an erase line such as **113** or **115** or **117** is connected to the erase gate of each cells in a row. An erase decoder **119** decodes an address on the internal address bus **111** and selectively connects the erase voltage V_{EG} on input line **121** to an erase line. This allows each row of cells to be addressed independently, such as the row **76** being simultaneously (Flash) erased by proper voltages applied to their erase gates through erase line **113**. In this case, the Flash cell consists of one row of memory cells. However, other Flash cell's implementations are possible and most applications will provide for simultaneous erasing of many rows of cells at one time.

Flash EEprom System

The addressable EEprom array **60** in FIG. **4** forms part of the larger multi-state Flash EEprom system of the present invention as illustrated in FIG. **5**. In the larger system, an EEprom integrated circuit chip **130** is controlled by a controller **140** via an interface **150**. The controller **140** is itself in communication with a central microprocessor unit **160**.

The EEprom chip **130** comprises the addressable EEprom array **60**, a serial protocol logic **170**, local power control circuits **180**, and various programming and reading circuits **190**, **200**, **210**, **220**, **230** and **240**.

The controller **140** controls the functioning of the EEprom chip **130** by supplying the appropriate voltages, controls and timing. Tables **1** and **2** shows typical examples of voltage conditions for the various operational modes of the EEprom cell. The addressable EEprom array **60** may be directly powered by the controller **140** or, as shown in FIG. **5**, be further regulated on chip by the local power control **180**. Control and data linkages between the controller **140** and the chip **130** are made through the serial in line **251** and the serial out line **253**. Clock timing is provided by the controller via line **255**.

In a typical operation of the EEprom chip **130**, the controller **140** will send a serial stream of signals to the chip **130** via serial in line **251**. The signals, containing control, data, address and timing information, will be sorted out by the serial protocol logic **170**. In appropriate time sequence, the logic **170** outputs various control signals **257** to control the various circuits on the chip **130**. It also sends an address via the internal address bus **111** to connect the addressed cell to voltages put out from the controller. In the meantime, if the operation is programming, the data is staged for programming the addressed cell by being sent via a serial data line **259** to a set of read/program latches and shift registers **190**.

Read Circuits and Techniques Using Reference Cells

To accurately and reliably determine the memory state of a cell is essential for EEprom operations. This is because all the basic functions such as read, erase verify and program verify depend on it. Improved and novel read circuits **220** for the EEprom chip **130** and techniques of the present invention make multi-state EEprom feasible.

As discussed in connection with FIG. **3**, the programmed charge placed on the floating gate **23'** determines the programmed threshold voltage V_{T1} of the cell. Generally, V_{T1} increases or decreases with the amount of negative charge on the floating gate **23'**. The charge can even be reduced to a positive value (depletion mode) where V_{T1} decreases below V_{T2} and even becomes negative. The maximum and minimum values of V_{T1} are governed by the dielectric strength of the device material. The span of V_{T1} defines a threshold voltage window in which memory states may be implemented.

Copending patent application Ser. No. 204,175, discloses an EEprom cell with memory states defined within a maximized window of threshold voltage V_{T1}. The full threshold voltage window includes the negative region of the threshold voltage, in addition to the usual positive region. The increased window provides more memory space to implement multi-state in an EEprom cell.

FIGS. **6** and **7** respectively illustrates the manner in which the threshold voltage window is partitioned for a 2-state memory and a 4-state memory cell. (Of course it is also possible to partition the window for a 3-state memory or even for a continuum of states in an analog, rather than digital memory).

Referring first to FIG. **6**, the solid curve **343** shows V_{T1} as a function of programming time. The threshold voltage window is delimited by the minimum and maximum values of V_{T1}, represented approximately by the Erase state level **345** and the Fully Program state level **347** respectively. The 2-state memory is implemented

by partitioning the window into two halves **346**, **348** using a breakpoint threshold level **349**. Thus, the cell may be considered to be in memory state **0** (or state **1**) if the cell is programmed with a V_{TI} within region **346** (or region **348**) respectively.

A typical erase/program cycle begins with erase which reduces the threshold voltage of the cell to its Erase state level **345**. Subsequent repetitive programming is used to increase the threshold voltage V_{TI} to the desired level. Rather than continuously applying programming voltages to the addressed cell for some fixed period of time corresponding to the state to which the cell is to be programmed, it is preferable to apply programming voltages in repetitive short pulses with a read operation occurring after each pulse to determine when it has been programmed to the desired threshold voltage level, at which time the programming terminates. The programming voltages and duration of the pulses are such that the pulses advance V_{TI} across the various regions rapidly but each pulse is sufficiently fine to not overshoot any of the regions. This minimizes voltage and field related stresses on the cell, and therefore improves its reliability.

FIG. **7A** illustrates the 4-state case where the threshold voltage window is partitioned into four regions **351**, **353**, **355**, **357** by breakpoint levels **352**, **354**, **356** respectively. The cell is considered to be in state "3" or "2" or "1" or "0" if its V_{TI} is programmed to be within corresponding regions **351** or **353** or **355** or **357** respectively. A 4-state cell is able to store two bits of data. Thus, the four states may be encoded as (1,1), (1,0), (0,1) and (0,0) respectively.

In general, if each EEprom cell is to store K states, the threshold window must be partitioned into K regions with at least $K-1$ threshold levels. Thus, only one breakpoint level is required for a 2-state memory cell, and three breakpoint levels are required for a 4-state cell.

In principle, a threshold voltage window may be partitioned to a large number of memory states. For example, for an EEprom device with a maximum threshold window of 16 V, it may be partitioned into thirty-two states each within an approximately half volt interval. In practice, prior art EEprom devices have only stored two states or one bit per cell with diminished reliability and life. Apart from operating with a smaller threshold window, prior devices fail to solve two other problems inherent in EEprom devices. Both problems relate to the uncertainty in the amount of charge in the floating gate and hence the uncertainty in the threshold voltage V_{TI} programmed into the cell.

The first problem has to do with the endurance-related stress the device suffers each time it goes through an erase/program cycle. The endurance of a Flash EEprom device is its ability to withstand a given number of program/erase cycles. The physical phenomenon limiting the endurance of prior art Flash EEprom devices is trapping of electrons in the active dielectric films of the device. During programming, electrons are injected from the substrate to the floating gate through a dielectric interface. Similarly, during erasing, electrons are extracted from the floating gate to the erase gate through a dielectric interface. In both cases, some of the electrons are trapped by the dielectric interface. The trapped electrons oppose the applied electric field in subsequent program/erase cycles thereby causing the programmed V_{TI} to shift to a lower value and the erased V_{TI} to shift to a higher value. This can be seen in a gradual closure in the voltage "window" between the "0" and "1" states of prior art devices as shown in FIG. **8A**. Beyond approximately 1×10^4 program/erase cycles the window closure can become sufficiently severe to cause the reading circuitry to malfunction. If cycling is continued, the device eventually experiences catastrophic failure due to a ruptured dielectric. This typically occurs at between 1×10^6 and 1×10^7 cycles, and is known as the intrinsic breakdown of the device. In prior art EEprom devices the window closure is what limits the practical endurance to approximately 1×10^4 program/erase cycles. This problem is even more critical if multi-state memory is implemented, since more accurate placement of V_{TI} is demanded.

A second problem has to do with the charge retention on the floating gate. The charge on the floating gate tends to diminish somewhat through leakage over a period of time. This causes the threshold voltage V_{TI} to shift also to a lower value over time. FIG. **8B** illustrates the reduction of V_{TI} as a function of time. Over the life time of the device V_{TI} may shift by as much as 1 V. In a multi-state device, this could shift the memory by one or two states.

The present invention overcomes these problems and presents circuits and techniques to reliably program and read the various states even in a multi-state implementation.

The memory state of a cell may be determined by measuring the threshold voltage V_{TI} programmed therein. Alternatively, as set forth in co-pending patent application, Ser. No. 204,175, the memory state may conveniently be determined by measuring the differing conduction in the source-drain current I_{DS} for the different states. In the 4-state example, FIG. **7A** shows the partition in the threshold voltage window. FIG. **7B**, on the other hand, illustrates typical values of I_{DS} (solid curves) for the four states as a function of the control gate voltage V_{CG}. With V_{CG} at 5 V, the I_{DS} values for each of the four conduction states can be distinguished by sensing with four corresponding current sensing amplifiers in parallel. Associated with each amplifier is a corresponding reference conduction states I_{REF} level (shown as broken curves in FIG. **8**). Just as the breakpoint threshold levels (see FIGS. **6** and **7A**) are used to demarcate the different regions in the threshold voltage window, the I_{REF} levels are used to do the same in the corresponding source-drain current window. By comparing with the I_{REF}'s, the conduction state of the memory cell can be determined. Co-pending patent application, Ser. No. 204,175 proposes using the same sensing amplifiers and I_{REF}'s for both programming and reading. This provides good tracking between the reference levels (broken curves in FIG. **89**) and the programmed levels (solid curves in FIG. **7B**).

In the improved scheme of the present invention, the I_{REF}'s are themselves provided by the source-drain currents of a set of EEprom cells existing on the same chip and set aside solely for this purpose. Thus, they act as master reference cells with their I_{REF}'s used as reference levels for the reading and programming of all other EEprom cells on the same chip. By using the same device as the EEprom cells to act as reference cells, excellent tracking with respect to temperature, voltage and process variations is achieved. Furthermore, the charge retention problem, important in multi-state implementation, is alleviated.

Referring to FIG. 9A, one such master reference cell **400** is shown with its program and read paths. The reference cells erase and program module **410** serves to program or re-program each such reference cell **400**. The module **410** includes program and erase circuits **411** with a programming path **413** connected to the drain of the master reference cell **400**. The circuits **411** are initiated by addresses decoded from the internal bus **111** by a program decoder **415** and an erase decoder **417** respectively. Accordingly, programming voltages or erasing voltages are selectively supplied each reference cell such as cell **400**. In this way, the reference level in each reference cell may be independently set or reprogrammed. Typically, the threshold level of each reference cell will be factory-programmed to the optimum level appropriate for each batch of chips produced. This could be done by comparison with an external standard reference level. By software control, a user also has the option to reset the reference threshold levels.

Once the reference threshold voltage V_{TI} or reference drain-source current I_{REF} is programmed into each reference cell **400**, it then serves as a reference for the reading of an addressed memory cell such as cell **420**. The reference cell **400** is connected to a first leg **403** of a current sensing amplifier **410** via a clocked switch **413**. A second leg **415** of the amplifier is essentially connected to the addressed memory cell **420** whose programmed conduction state is to be determined. When cell **420** is to be read, a control signal READ will enable a switch **421** so that the cell's drain is connected to the second leg **415**. The sense amplifier **410** supplies voltage via V_{CC} to the drains of both the master reference cell **400** and the addressed cell **420**. In the preferred embodiment, the amplifier has a current mirror configuration such that any differential in currents through the two legs **403** and **415** results in the voltage in the second leg **415** being pulled up towards V_{CC} or down towards V_S. Thus, the node at the second leg **415** is respectively HIGH (or LOW) when the source-drain current I_{DS} for the addressed cell **420** is less (or more) than I_{REF} through the master reference cell **400**. At the appropriate time controlled by a clocked switch **423**, the sensed result at the second leg **415** may be held by a latch **425** and made available at an output line **427**. When I_{DS} is less than I_{REF}, a HIGH appears at the output line **427** and the addressed cell **420** is regarded as in the same conduction state as the master reference cell **400**.

In the preferred embodiment, a voltage clamp and fast pull-up circuit **430** is also inserted between the second leg **415** and the drain **431** of the addressed cell **420**. The circuit **430** serves to keep the drain voltage V_D at a maximum of 1.5 V-2.0 V when it is charging up in the case of lower I_{DS}. It also prevents V_D from pulling too low in the case of higher I_{DS}.

In general, if each memory cell is to store K states, then at least K−1, or preferably K reference levels need be provided. In one embodiment, the addressed cell is compared to the K reference cells using k sense amplifiers in parallel. This is preferable for the 2-state case because of speed, but may spread the available current too thin for proper sensing in the multi-state case. Thus, for multi-state case, it is preferable to compare the addressed cell with the K reference cells one at a time in sequence.

FIG. 9B illustrates more explicitly the multi-state reading configuration. The K reference cells such as **431**, **433**, **435** are connected to the sense amplifier **440** via the amplifier's first leg **441**. The connection is time-multiplexed by clocked switches such as **451**, **453**, **455** respectively. The second leg **457** of the sense amplifier is connected to the addressed cell as in FIG. 9A. The sensed signal at the second leg **457** is time-selectively latched by clocked switches such as **461**, **463**, **465** onto such latches **471**, **473**, **475**.

FIGS. 9C(1)-9C(8) illustrates the timing for multi-state read. When the signal READ goes HIGH, a switch **421** is enabled and the addressed memory cell is connected to the second leg **457** of the sense amplifier **440** (FIG. 9C(1)). The clocks' timing is given in FIGS. 9C(2)-9C(4). Thus, at each clock signal, the sense amplifier sequentially compares the addressed cell with each of the reference cells and latches each results. The latched outputs of the sense amplifier are given in FIGS. 9C(5)-9C(7). After all the K output states of the sense amplifier **440** are latched, they are encoded by a K-L decoder **480** ($2^L \geqq K$) (FIG. 9C(8)) into L binary bits.

Thus, the multiple threshold levels are provided by a set of memory cells which serves as master reference cells. The master reference cells are independently and externally erasable and programmable, either by the device manufacturer or the user. This feature provides maximum flexibility, allowing the breakpoint thresholds to be individually set within the threshold window of the device at any time. By virtue of being the same device as that of the memory cells, the reference cells closely track the same variations due to manufacturing processes, operating conditions and charge retention problems. The independent programmability of each threshold level at will allows optimization and fine-tuning of the partitioning of the threshold window to make multi-state memory viable. Furthermore, it allows post-manufacture configuration for either 2-state or multi-state memory from the same device, depending on user need or device characteristics at the time.

Another aspect of the present invention provides improved multi-state sensing of an addressed memory cell. As discussed in connection with an earlier embodiment for sensing a mult-state memory, it is preferable to compare the cell's conduction current with all the reference conduction current levels (threshold levels) simultaneously or in parallel. For example, a 4-state memory cell has at least three reference current levels to demarcate the four states. Parallel sensing the state of the cell means simultaneous comparison of the cell's conduction current I_{CELL} versus each of the three reference current levels. This is faster than comparing with each of the three reference conduction levels sequentially. However, in the simpler embodiment described earlier, the conduction current of the addressed cell would be diluted by being divided up into three branches, one for each reference level comparison. Thus, a simple implementation of simultaneous or parallel multi-state sensing may be prohibited by the signal-to-noise ratio requirement of the sensing system, especially when there are many states involved.

FIG. 9D-FIG. 9I illustrate several embodiments of simultaneous multi-state sensing without the disadvantage of degrading the conduction current of the sensed cell. In each embodiment, a one-to-many current mirror is employed to reproduce a current into many copies so that each copy may be used to compare with a reference current level at the same time.

FIG. 9D illustrates a first embodiment of simultaneous multi-state sensing. A one-to-many current mir-

ror comprises a first transistor **910** on a first leg **920** and a second transistor **911, 912, . . . , 915** respectively on each branch **921, 922, . . . , 925** of a second leg. Whenever, a first current flows in the first leg **920**, the second transistor on each branch of the second leg behaves as a current source and supplies a reproduced current in its branch. The ratio of reproduced current to the first current scales according to the relative sizes of the second transistor **911, 912, . . . , 915** to the first transistor **910**.

In the present embodiment, all the transistors have the same size as denoted by the symbol "X" shown in FIG. **9D**. This results in a one-to-many current mirror in which the first current in the first leg **920** is identically reproduced in all branches **921, 922, . . . , 925** of the second leg. Thus, when the conduction current I_{CELL} of an addressed memory cell **420** flows through a read enabling switch **421** in the first leg **920**, the same current I_{CELL} is reproduced in the branches **921, 922, . . . , 925** of the second leg. This is achieved without dilution of I_{CELL}.

Once I_{CELL} is reproduced in each branch, it is compared to an associated reference current level. This is accomplished by also driving each branch with a second current source **931, 932, . . . , 935** in-line with the first current source **911, 912, . . . , 915** respectively. Each second current source or I_{REF} circuit **931, 932, . . . , 935** supplies respectively the predetermined reference current level such as I_{REF1} in line **941** of the first branch, I_{REF2} in line **942** of the second branch, . . . , and I_{REFk} in line **953** of the kth branch. The memory state is then determined by sensing the location of the I_{CELL} level relative to the I_{REF}'s. The sensed outputs for each state denoted by SA1, SA2, . . . , SAk in FIG. **9D** are respectively derived from a node **951** of the first branch, a node **952** of second branch, . . . , and a node **953** of the kth branch. The node in each branch is situated between the first and second current source. In general the two current sources are of opposite polarity. If the second current source **931, 932, . . . , 935** is an n-channel transistor connected to V_S on one end, then the first current source is a p-channel transistor **911, 912, . . . , 915** connected to V_{CC} on the other end. Depending on the relative levels of I_{CELL} and I_{REF} in the two current sources, the node is either pulled up towards V_{CC} (typically, 5 V) or down towards V_S (typically, 0 V). For example, in the first branch, a current I_{CELL} is reproduced in line **921** and a current I_{REF1} is supplied in line **941**. The node **951** is respectively HIGH (or LOW) when I_{CELL} is greater than (or less than) I_{REF1}. Thus, a memory state having an I_{CELL} that lies between I_{REF1} and I_{REF2} would only have the node **951** HIGH, thereby resulting in a multi-state output (SA1, SA2, . . . , SAk)=(0, 1, . . . , 1).

In general, each I_{REF} circuit **931, 932, . . . , 935** can be a current source circuit pre-adjusted to supply the various reference current levels I_{REF1}, I_{REF2}, . . . , I_{REF3}.

FIG. **9E** illustrates one embodiment in EEprom applications in which each I_{REF} circuit **931, 932, . . . , 935** is provided respectively by a reference cell **431, 432, . . . , 435** which is itself an EEprom cell similar to that described in connection with FIGS. **9A** and **9B**. Thus the reference cell may be applicable as a master reference cell or a local reference cell in which a reference conduction current level may be programmed.

FIG. **9F** illustrates a preferred implementation where each I_{REF} circuit is not provided directly by a reference cell, but rather by a reproduction of it. This enables a chunk (e.g., 64) of memory cells to share the same reference cell for simultaneous sensing. A transistor **961, 962, . . . , 965** respectively in each of the I_{REF} circuit **931, 932, . . . , 935** serves as a current source for supplying the reproduced reference current level from each of the reference cells **431, 432, . . . , 435**. Each transistor is controlled by a reference voltage REF1, REF2, . . . , REFk at its gate to produce the required reference current levels I_{REF1}, I_{REF2}, . . . , I_{REF3}. Each reference voltage is furnished by a REF circuit **971, . . . , . . . , 975**. An alternative view is that each transistor **961, 962, . . . , 965** and the associated REF circuit **971, . . . , . . . , 975** form a double current mirror circuit by which the reference current of each reference cell **431, 432, . . . , 435** is reproduced as the conduction current of the transistor **961, 962, . . . , 965**. Considering the I_{REF1} circuit **931** as a representative, it comprises the transistor **961** as a current source for I_{REF1}. The I_{REF1} level is obtained as a reproduction of the conduction current of the reference cell **431**. The reference cell **431** supplies a reference current I_{REF1} to a first leg **976** of the first current mirror that gets reproduced in a second leg **977** thereof. The second leg **977** of the first current mirror is interconnected with a first leg of the second current mirror. Thus the reproduced reference current is in turn reproduced in the second leg **941** of the second mirror by the transistor **961**. Generally, the two current mirrors are of opposite polarity. For example, when the REF1 cell **431** is an n-channel transistor, the first current mirror comprises of two p-channel transistors **981** and **982** of equal size "X", and the second current mirror comprises of two n-channel transistors **983** and **961** of equal size "W".

FIG. **9G** illustrates another embodiment in which the different I_{REF} levels supplied by the second current source of each branch are all generated from one reference circuit **976**. The reference circuit **976** provides a reference voltage that is applied to every gate of the transistor **961, 962, . . . , 965** of each branch respectively. As in the embodiment illustrated in FIG. **9F**, the reference voltage serves to turn on the transistors. However, the different levels of I_{REF}'s across the branches are now obtained by adjusting the size of the transistors **961, 962, . . . , 965**. For example, as illustrated in FIG. **9G**, the transistors **961, 962, . . . , 965** respectively have sizes of I*W, J*W, . . . , K*W, where I:J: . . . :K are respectively in the same ratios as I_{REF1}:I_{REF2}: . . . :I_{REFk}. The single reference circuit **976** may be a constant voltage source or a circuit involving a reference cell similar to the REF circuit **971** in FIG. **9F**. This applies under the normal current mirroring condition in which the transistors in each branch such as M81 and **961** are biased in the saturation region.

FIG. **9H** illustrates another embodiment in which all the second current sources are the same across the branches but I_{CELL} is reproduced by the first current source into each branch with levels scaled according to the gradation of the reference current levels. The scaling is effected by adjusting the size of each second transistor **911, 912, . . . , 915**. For example, as illustrated in FIG. **9H**, the second transistors **911, 912, . . . , 915** respectively have sizes of I*X, J*X, . . . , K*X, where X is the size of the first transistor **910** in the first leg **920** and I:J: . . . :K are respectively in the same ratios as I_{REF1}:I_{REF2}: . . . :I_{REFk}. Thus, only one REF circuit **976** is used across the branches, and furthermore, the sizes of all the transistors **961, 962, . . . , 965** are now identical. The single reference circuit **976** may be a constant volt-

age source or may be a circuit involving a reference cell similar to the REF circuit **971** in FIG. **9F**. In one implementation, the reference circuit **976** is such that each second current source **961, 962, . . . , 965** is made to supply a current equal to the highest reference current level I_{REFk}. The order of the outputs from the nodes is reversed relative to the embodiments illustrated in FIGS. **9D–9G**.

FIG. **9I** illustrates yet another embodiment of simultaneous multi-state sensing with a circuit similar to that in FIG. **9G**, except the identities of the address memory cell and the IREF circuit are interchanged. In other words, in each branch, the second current source such as **931, 932, . . . , 935** now supplies a reproduced I_{CELL}. This is achieved by means of an addressed memory cell circuit **977** feeding a reference voltage MC to every gate of the transistor **961, 962, . . . , 965** of each branch respectively. The circuit **977** is similar to the REF1 circuit **971** in FIG. **9F**, except the REF1 CELL **431** is now replaced by the addressed memory cell **420**. Similarly, the first current source such as **911, 912, . . . , 915** now supplies respectively I_{REF1}, I_{REF2}, . . . , I_{REFk}. The various I_{REF}'s are obtained by a scaled reproduction of the current of an IREF0 circuit **978**. The scaling is effected by adjusting the size of each second transistor **911, 912, . . . , 915** in the one-to-many current mirror. For example, as illustrated in FIG. **9I**, the second transistors **911, 912, . . . , 915** respectively have sizes of I*X, J*X, . . . , K*X, where X is the size of the first transistor **910** in the first leg **920** and 1:1:J: . . . :K are respectively in the same ratios as I_{REF0}:I_{REF1}:I_{REF2}: . . . :I_{REFk}. In general, the IREF0 circuit **978** may be any current source which supplies a current level of I_{REF0}. In one embodiment, the IREF0 circuit is an EEprom cell programmable with a reference current level, similar to that described in connection with FIGS. **9A** and **9B**.

Another important feature of the present invention serves to overcome the problems of endurance-related stress. As explained previously, the erase, program and read characteristics of each memory cell depends on the cumulated stress endured over the number of program/erase cycles the cell has been through. In general, the memory cells are subjected to many more program/erase cycles than the master reference cells. The initially optimized reference levels will eventually become misaligned to cause reading errors. The present underlying inventive concept is to have the reference levels also reflect the same cycling suffered by the memory cells. This is achieved by the implementation of local reference cells in addition to the master reference cells. The local reference cells are subjected to the same program/erase cycling as the memory cells. Every time after an erase operation, the reference levels in the master reference cells are recopied into the corresponding set of local reference cells. Memory cells are then read with respect to the reference levels of the closely tracking local reference cells. In this way, the deviation in cell characteristics after each program/erase cycle is automatically compensated for. The proper partitioning of the transforming threshold window is therefore maintained so that the memory states can be read correctly even after many cycles.

FIG. **10** illustrates the local cells referencing implementation for Flash EEprom. In the Flash EEprom array **60** (FIG. **4**), each group of memory cells which is collectively erased or programmed is called a sector. The term "Flash sector" is analogous to the term "sector" used in magnetic disk storage devices and they are used interchangeably here. The EEprom array is grouped into Flash sectors such as **501, 503** and **505**. While all memory cells in a Flash sector suffer the same cycling, different Flash sectors may undergo different cycling. In order to track each Flash sector properly, a set of memory cells in each Flash sector is set aside for use as local reference cells. For example, after the Flash sector **503** has been erased, the reference levels in the master reference cells **507** are re-programmed into the local reference cells associated with the Flash sector **503**. Until the next erase cycle, the read circuits **513** will continue to read the memory cells within the Flash sector **503** with respect to the re-programmed reference levels.

FIGS. **11(1)–11(7)** illustrates the algorithm to re-program a sector's reference cells. In particular, FIGS. **11(1)–11(3)** relate to erasing the sector's local reference cells to their "erased states". Thus in FIG. **11(1)**, a pulse of erasing voltage is applied to all the sector's memory cells including the local reference cells. In FIG. **11(2)**, all the local reference cells are then read with respect to the master references cells to verify if they have all been erased to the "erased state". As long as one cell is found to be otherwise, another pulse of erasing voltage will be applied to all the cells. This process is repeated until all the local reference cells in the sector are verified to be in the "erased" state (FIG. **11(3)**).

FIGS. **11(4)–11(7)** relate to programming the local reference cells in the sector. After all the local reference cells in the sector have been verified to be in the "erased" state, a pulse of programming voltage is applied in FIG. **11(4)** only to all the local reference cells. This is followed in FIG. **11(5)** by reading the local reference cells with respect to the master reference cells to verify if every one of the local reference cells is programmed to the same state as the corresponding master reference cell. For those local reference cells not so verified, another pulse of programming voltage is selectively applied to them alone (FIG. **11(6)**). This process is repeated until all the local reference cells are correctly verified (FIG. **11(7)**) to be programmed to the various breakpoint threshold levels in the threshold window.

Once the local reference cells in the sector have been re-programmed, they are used directly or indirectly to erase verify, program verify or read the sector's addressed memory cells.

FIG. **12A** illustrates one embodiment in which the local reference cells are used directly to read or program/erase verify the sector's memory cells. Thus, during those operations, a parallel pair of switches **525** is enabled by a READ signal and the sense amplifier **440** will read the sector's addressed memory cells **523** with respect to each of the sector's local reference cells **525**. During program/erase verify of the local reference cells (as illustrated in FIG. **11**), another parallel pair of switches **527** enables reading of the local reference cells **525** relative to the master reference cells **529**.

FIG. **12B** illustrates the algorithm for using the local reference cells directly to read or program/erase verify the sector's addressed memory cells.

FIG. **13A** illustrates an alternative embodiment in which the local reference cells are used indirectly to read the addressed memory cells. First the master reference cells are erased and programmed each to one of the desired multiple breakpoint thresholds within the threshold window. Using these master reference thresholds the local reference cells within an erased sector of

cells are each programmed to one of the same desired multiple breakpoint thresholds. Next the addressed cells in the sector are programmed (written) with the desired data. The reading sequence for the addressed cells in the sector then involves the steps illustrated in FIG. **13A**.

First each of the local reference cells **525** is read relative to the corresponding master reference cell **531**. This is effected by an enabling READ **1** signal to a switch **533** connecting the local reference cells **525** to the second leg **457** of the sense amplifier **440** with the master reference **531** connected to the first leg **441** of the sense amplifier. Auxiliary current source circuits associated with each master reference cell are now used to optimally bias the current through the first leg **441** of the sense amplifier to match the current in the second leg **457**. After the bias adjustment operation is completed for all breakpoint threshold levels the addressed cells in the sector are read relative to the bias-adjusted master reference cells. This is effected by disabling READ **1** to **533** and enabling READ signal to switch **535**. The advantage of this approach is that any variations in V_{CC}, temperature, cycling fatigue or other effects which may, over time, cause threshold deviations between the master reference cells and the addressed cells is eliminated prior to reading, since the local reference cells (which track threshold deviations of the addressed cells) are used to effectively readjust the breakpoint thresholds of the master reference cells. For example, this scheme permits programming of the addressed cells when the master reference cells are powered with $V_{CC}=5.5$ V and subsequently reading the addressed cells with the master reference cells powered at $V_{CC}=4.5$ V. The difference of 1 volt in V_{CC}, which would normally cause a change in the value of the breakpoint thresholds, is neutralized by using the local reference cells to bias adjust the master reference cells to counteract this change at the time of reading.

FIGS. **13B** and **13C** show in more detail one embodiment of the current biasing circuits such as **541, 543, 545** for the master reference cells **551, 553, 555**. Each biasing circuit acts as a current shunt for the current in the master reference cell. For example, the circuit **541** is tapped to the drain of the master reference cell **551** through the line **561**. It modifies the current in line **562** to the sense amplifier (first leg) either by sourcing current from V_{CC} or draining current to V_{SS}. In the former case, the current in the line **562** is reduced, and otherwise for the latter case. As biasing is being established for the master reference **551**, any inequality in the currents in the two legs of the sense amplifier can be communicated to outside the chip. This is detected by the controller (see FIG. **5**) which in turn programs the biasing circuit **541** via the internal address bus **111** to subtract or add current in the line **562** in order to equalize that of the local reference.

FIG. **13C** illustrates an embodiment of the biasing circuit such as the circuit **541**. A bank of parallel transistors such as **571, 573, 575** are all connected with their drains to V_{CC}, and their sources via switches such as **581, 583, 585** to the line **561**. By selectively enabling the switches, different number of transistors may be used to subtract various amount of current from line **562**. Similarly, another bank of parallel transistors such as **591, 593, 595** are all connected with their sources to V_{SS}, and their drains via switches such as **601, 603, 605** to the line **561**. By selectively enabling the switches, different number of transistors may be used to add various amount of current to line **562**. A decoder **609** is used to decode address from the internal address bus **111** to selectively enable the switches. The enabling signals are stored in latches **611, 613**. In this way every time a sector is read, the master reference cells are re-biased relative to the local reference cells, and used for reading the memory cells in the sector.

FIGS. **13D(1)-13D(4)** illustrate the read algorithm for the alternative embodiment. The sector must previous had its local reference cells programmed and verified relative to the master reference cells (FIG. **13D(1)**). Accordingly, each of the master reference cells is then read relative to the local reference cells (FIG. **13D(2)**). The master reference cells are biased to equalize the current to that of the corresponding local reference cells (FIG. **13D(3)**). Subsequently, the memory cells in the sector are read relative to the biased master reference cells (FIG. **13D(4)**).

The read circuits and operation described are also employed in the programming and erasing of the memory cells, particularly in the verifying part of the operation. As described previously, programming is performed in small steps, with reading of the state programmed in between to verify if the desired state has been reached. As soon as the programmed state is verified correctly, programming stops. Similarly, erasing is performed in small steps, with reading of the state of erase in between to verify if the "erased" state has been reach. Once the "erased" state is verified correctly, erasing stops.

As described previously, only $K-1$ breakpoint threshold levels are required to partition the threshold window into K regions, thereby allowing the memory cell to store K states. According to one aspect of the present invention, however, in the multi-state case where the threshold window is more finely partitioned, it is preferable to use K threshold levels for K state. The extra threshold level is used to distinguish the "erased" state from the state with the lowest threshold level. This prevents over-erasing and thus over-stressing the cell since erasing will stop once the "erased" state is reached. The selective inhibition of individual cells for erase does not apply to the Flash EEprom case where at least a sector must be erased each time. It is suitable those EEprom arrays where the memory cells can be individually addressed for erase.

According to another feature of the invention, after a memory cell has been erased to the "erased" state, it is programmed slightly to bring the cell to the state with the lowest threshold level (ground state) adjacent the "erased" state. This has two advantages. First, the threshold levels of the ground state of all the memory cells, being confined between the same two breakpoint threshold levels, are well-defined and not widely scattered. This provide an uniform starting point for subsequent programming of the cells. Secondly, all cells get some programming, thereby preventing those cells which tend to have the ground state stored in them, for example, from losing track with the rest with regard to program/erase cycling and endurance history.

On Chip Program Verify

As mentioned before, programming of an EEprom cell to a desired state is preferably performed in small steps starting from the "erase" state. After each programming step, the cell under programming is read to verify if the desired state has been reached. If it has not, further programming and verifying will be repeated until it is so verified.

Referring to the system diagram illustrated in FIG. 5, the EEprom chip 130 is under the control of the controller 140. They are linked serially by the serial in line 251 and serial out line 253. In prior art EEprom devices, after each programming step, the state attained in the cell under programming is read and sent back to the controller 140 or the CPU 160 for verification with the desired state. This scheme places a heavy penalty on speed especially in view of the serial link.

In the present invention, the program verification is optimized by programming a chunk (typically several bytes) of cells in parallel followed by verifying in parallel and on chip. The parallel programming is implemented by a selective programming circuit which disables programming of those cells in the chunk whose states have already been verified correctly. This feature is essential in a multi-state implementation, because some cells will reach their desired state earlier than others, and will continue pass the desired state if not stopped. After the whole chunk of cells have been verified correctly, logic on chip communicates this fact to the controller, whereby programming of the next chunk of cells may commence. In this way, in between each programming step data does not need to be shuttled between the EEprom chip and the controller, and program verification speed is greatly enhanced.

FIG. 14 illustrates the program and verify paths for a chunk of n cells in parallel. The same numerals are used for corresponding modules in the system diagram of FIG. 5. The EEprom array 60 is addressed by N cells at a time. For example, N may be 64 cells wide. In a 512 bytes Flash sector, consisting of 4 rows of 1024 cells, there will be 64 chunks of 64 cells. The source multiplexer 107 selectively connects the N sources of one addressed chunk of cells to the source voltage V_S in line 103. Similarly, the drain multiplexer 109 selectively makes the N drains of the chunk accessible through an N-channel data path 105. The data path 105 is accessed by the program circuit with inhibit 210 during programming and by read circuits 220 during reading, program verifying or erase verifying.

Referring again to the system diagram in FIG. 5, programming is under the control of the controller 140. The data to be programmed into the sector is sent chunk by chunk. The controller first sends a first chunk of N*L serial data bits together with addresses, control and timing information to the EEprom chip 130. L is the number of binary bits encoded per memory cell. For example, L=1 for a 2-state cell, and L=2 for a 4-state cell. Thus if N=64 and L=2, the chunk of data bits will be 128 bits wide. The N*L data bits are stored in latches and shift registers 190 where the serial bits are converted to N*L parallel bits. These data will be required for program verify in conjunction with the read circuits 220, bit decoder 230, compare circuit 200 and the program circuit with inhibit 210.

The program algorithm for a chunk of N cells is best described by referring to both the system diagram of FIG. 5 and FIGS. 15(1)-15(7) which illustrate the algorithm itself. As mentioned in an earlier section, prior to programming the sector, the whole sector must be erased and all cells in it verified to be in the "erased" state (FIG. 15(1)). This is followed in FIG. 15(2) by programming the sector local reference cells (as shown in FIGS. 11(1)-(3)). In FIG. 15(3), the N*L bits of parallel data is latched in latches 190. In FIG. 15(4), the read circuits 220 access the N-channel data path 105 to read the states in the N chunk of cells. The read algorithm has already been described in conjunction with FIG. 12B or FIG. 13D. The N-cell reads generates N*K (K=number of states per cell) output states. These are decoded by bit decoder 230 into N*L binary bits. In FIG. 15(5), the N*L read bits are compared bit by bit with the N*L program data bits from latches 190 by compare circuit 200. In FIG. 15(6), if any read bit fails to compare with the program data bit, a further programming voltage pulse from the program circuit 210 is applied simultaneously to the chunk of cells. However, an inhibit circuit within the program circuit 210 selectively blocks programming to those cells whose bits are correctly verified with the programmed data bits. Thus, only the unverified cells are programmed each time. Programming and verification are repeated until all the cells are correctly verified in FIG. 15(7).

FIG. 16 shows one embodiment of the compare circuit 200 of FIG. 5 in more detail. The circuit 200 comprises N cell compare modules such as 701, 703, one for each of the N cells in the chunk. In each cell compare module such as the module 701, the L read bits (L=number of binary bits encoded for each cell) are compared bit by bit with the corresponding program data bits. This is performed by L XOR gates such as 711, 713, 715. The output of these XOR gates pass through an NOR gate 717 such that a "1" appears at the output of NOR gate 717 whenever all the L bits are verified, and a "0" appears when otherwise. When the control signal VERIFY is true, this result is latched to a latch 721 such that the same result at the output of NOR gate 717 is available at the cell compare module's output 725. The compare circuit 200 performs the comparisons of L bits in parallel. The N compare module's outputs such as 725, 727 are available at an N-channel output line 731 to be fed to the program circuit with inhibit 210 of FIG. 5.

At the same time, the N outputs such as 725, 727 are passed through an AND gate 733 so that its single output 735 results in a "1" when all N cells are verified and a "0" when otherwise. Referring also to FIG. 5, the single output 735 is used to signal the controller 140 that all N cells in the chunk of data have been correctly verified. The signal in output 735 is sent through the serial out line 253 via AND gate 240 during a VERIFY operation.

At power-up or at the end of program/verify of a chunk of data, all cell compare module's outputs such as 725, 727 are reset to the "not-verified" state of "0". This is achieved by pulling the node 726 to V_{SS} (0 V) by means of the RESET signal in line 727 to a transistor 729.

FIG. 17 shows one embodiment of the program circuit with inhibit 210 of FIG. 5 in more detail. The program circuit 210 comprises N program with inhibit modules such as 801, 803. As illustrated in Table 1 and 2, in order to program the N cells, a voltage V_{PD} must be applied to each of the N cells' drain and a voltage V_{PG} applied to the control gates. Each program module such as 801 serves to selectively pass V_{PD} on a line 805 to one of the drains through the one of the N-channel data path 105. Since V_{PD} is typically about 8 V to 9 V which is higher than V_{CC}, the latter cannot be used to turn on the transistor switch 807. Rather the higher voltage V_{CG} (about 12 V) is used to enable switch 807. V_{CG} in line 801 is itself enabled by an AND gate when both the program control signal PGM in line 813 is true and the signal in line 731 is a "0". Since the signal in line 731 is from the output of the cell compare module 701

shown in FIG. **16**, it follows that V_{PD} will be selectively passed onto those cells which are not yet verified. In this way, every time a programming pulse is applied, it is only applied to those cells which have not yet reached their intended states. This selective programming feature is especially necessary in implementing parallel programming and on chip verification in the multi-state case.

Variable Control of Voltage to the Control Gate

The system diagram of FIG. **5** in conjunction with Tables **1** and **2** illustrate how various voltages are applied to the EEprom array **60** to perform the basic functions of the EEprom. Prior art EEprom devices only allow the voltage supplied to the control gate V_{CG} to assume one of two voltages, namely V_{CC} or the higher programming voltage of about 12 V.

In another aspect of the present invention, the voltage supplied to the control gate V_{CG} is allowing to be independently and continuously variable over a wide range of voltages. This is provided by V_{PG} from the controller **140**. In particular V_{CG} in a line **83** is fed from V_{PG} which is in turn supplied by the controller from a line **901**. Table **2** shows V_{PG} to assume various voltages under different functions of the EEprom.

The variability of V_{CG} is particularly advantageous in program and erase margining schemes. In program margining, the read during program verify is done with V_{CG} at a slightly higher voltage than the standard V_{CC}. This helps to place the programmed threshold well into the state by programming past the breakpoint threshold level with a slight margin. In erase verify, the cell is verified with a somewhat reduced V_{CG} to put the cell well into the "erased" state. Furthermore, margining can be used to offset the charge retention problem described earlier (FIG. **8B**).

As mentioned before, prior art EEproms typically employ V_{CC} to feed V_{CG} during program or erase verify. In order to do margining, V_{CC} itself needs to be ramped up or reduced. This practice produces inaccurate results in the reading circuits since they are also driven by V_{CC}.

In the present invention, the variability of V_{CG} independent of voltages supplied to the reading circuit produce more accurate and reliable results.

Furthermore, the wide range of V_{CG} is useful during testing and diagnostic of the EEprom. It allows the full range of the programmed cell's threshold to be measured easily by continuing to increase V_{CG} (up to the maximum limited by the device's junction breakdown).

While the embodiments of this invention that have been described are the preferred implementations, those skilled in the art will understand that variations thereof may also be possible. Therefore, the invention is entitled to protection within the full scope of the appended claims.

What is claimed is:

1. In an integrated circuit memory system having an array of a plurality of addressable semiconductor electrically erasable and programmable memory (EEprom) cells of the type having a source, a drain, a control gate, a floating gate capable of retaining a charge level programmed into it during use of the memory system, resulting in a definite memory state having a corresponding threshold of conduction relative to a set of predetermined threshold levels used to demarcate memory states, and an erase electrode capable of removing charge from said floating gate, said array of EEprom cells being organized into one or more sectors of cells, where cells in each sector are erasable simultaneously, and said memory system including a reading system for determining the programmed state of an addressed cell in a given sector, said reading system comprising:

a set of sector reference memory cells associated with each sector, each set of sector reference memory cells being made up of memory cells from the sector associated therewith, thereby being electrically erasable along with its associated sector, and each set being programmable and having the set of predetermined threshold duplicated therein;

reprogramming means for duplicating the set of predetermined threshold to said set of sector reference memory cells after said set of sector reference memory cells has been erased along with its associated sector; and

means for comparing the addressed cell's programmed threshold relative to the set of predetermined thresholds duplicated in the set of sector reference memory cells associated with said given sector, thereby determining the memory state programmed in the addressed cell.

2. The integrated circuit memory system as in claim **1**, wherein the reading system is also part of a program verifying system during programming of the memory cells in which each addressed cell is programmed to a desired state by altering the threshold incrementally by repetitive sequence of programming and reading to verify the state programmed until the desired state is reached.

3. The integrated circuit memory system as in claim **1**, wherein the reading system is also part of an erase verifying system during erasing of the memory cells in which each addressed cell is erased to the erased state by altering the threshold incrementally by repetitive sequence of erasing and reading to verify the state erased until the erased state is reached.

4. The integrated circuit memory system according to claim **1**, which additionally comprises:

a set of master reference cells associated with the array for having the set of predetermined thresholds programmed therein, said set of master reference cells being constituted from EEprom cells of the array, thereby being electrically erasable and programmable; and wherein

said reprogramming means for each sector after erasure thereof duplicates the set of predetermined thresholds from the set of master reference cells to the associated set of sector reference memory cells.

5. The memory cell array reading system according to claim **4**, wherein said set of master reference cells constitutes at least one cell for programming a reference predetermined threshold therein, and the set of predetermined thresholds is obtainable by scaling said reference predetermined threshold.

6. The integrated circuit memory system according to claim **4**, wherein the charge level stored in each said master reference cell is electrically erasable and programmable from outside of said memory system.

7. In an integrated circuit memory system having an array of a plurality of addressable semiconductor electrically erasable and programmable memory (EEprom) cells of the type having a source, a drain, a control gate, a floating gate capable of retaining a charge level programmed into it during use of the memory system resulting in a memory state having a corresponding threshold of conduction, and an erase electrode capable

of removing charge from said floating gate, said array of EEprom cells being organized into one or more sectors of cells, where cells in each sector are erasable simultaneously, and said memory system including a reading system for determining the programmed threshold of an addressed cell relative to each of a set of predetermined thresholds used to demarcate memory states, said reading system comprising:

one or more sets of sector reference memory cells, each set having the set of predetermined thresholds programmed therein, and being constituted from a sector associated therewith, thereby being electrically erasable with its associated sector and being programmable;

a set of master reference cells associated with the array for having the set of predetermined thresholds programmed therein, and being constituted from EEprom cells of the array, thereby being electrically erasable and programmable;

reprogramming means for each sector after erasure thereof for duplicating the set of predetermined thresholds from the set of master reference cells to each sector's associated set of sector reference memory cells;

means for adjusting the set of predetermined thresholds from said set of master reference memory cells to substantially match that from the set of sector reference memory cells; and

reading means for comparing the threshold of the addressed cell to the set of adjusted thresholds, thereby determining the addressed cell's memory state.

8. In an integrated circuit memory system having an array of a plurality of addressable semiconductor electrically erasable and programmable memory (EEprom) cells of the type having a source, a drain, a control gate, a floating gate capable of retaining a charge level programmed into it during use of the memory system, resulting in a definite memory state having a corresponding threshold of conduction relative to at least two predetermined threshold levels used to demarcate memory states, and an erase electrode capable of removing charge from said floating gate, and said memory system including a reading system for determining the programmed state of an addressed cell, said reading system comprising:

at least two reference memory cells constituted from the array of EEprom cells that are each respectively programmed with a charge that corresponds to each of said at least two predetermined thresholds; and

means responsive to said at least two reference memory cells for comparing the charge level of an addressed cell with that of said reference memory cells, thereby determining relative to which of said at least two predetermined threshold levels of the addressed cell lies, whereby more than a single bit of data is stored and read from the addressed cell.

9. The system as in claim **8**, wherein the reading system is also part of a system for programming the memory cells in which each addressed cell is programmed to a desired state by altering the stored charge incrementally by repetitive sequence of programming and reading to verify the state programmed until the desired state is reached.

10. The system as in claim **8**, wherein the reading system is also part of an erasing system in which each addressed cell is erased to the erased state by altering the stored charge incrementally by repetitive sequence of erasing and reading to verify the state erased until the erased state is reached.

11. The memory cell reading system according to claim **8**, wherein said comparing means includes means for comparing said addressed cell with the at least two predetermined threshold levels of said at least two reference memory cells one at a time in sequence.

12. The memory cell reading system according to claim **8**, which additionally includes means for independently erasing and programming said at least two reference memory cells to said at least two predetermined threshold from outside of said memory.

13. In an array of a plurality of addressable semiconductor electrically erasable and programmable memory cells of the type having a source, a drain, a control gate, a floating gate capable of retaining a charge level programmed into it during use of the memory, and an erase electrode capable of removing charge from said floating gate, a system for reading the stored charge of an addressed cell within two ranges defined by one predetermined threshold level, comprising:

at least one reference memory cell constituted from the array of EEprom cells that is programmed with a charge that substantially corresponds to said predetermined threshold; and

means responsive to said reference memory cell for comparing the charge level of an addressed cell with that of said reference memory cell, thereby determining which of said two stored ranges that the stored charge of the addressed cell lies, whereby a single bit of data is stored and read from each of the addressed cells.

14. The system as in claim **13**, wherein the reading system is also part of a system for programming the memory cells in which each addressed cell is programmed to a desired state by altering the threshold incrementally by repetitive sequence of programming and reading to verify the state programmed until the desired state is reached.

15. The system as in claim **13**, wherein the reading system is also part of an erasing system in which each addressed cell is erased to the erased state by altering the threshold incrementally by repetitive sequence of erasing and reading to verify the state erased until the erased state is reached.

16. In an array of a plurality of addressable semiconductor electrically erasable and programmable memory cells of the type having a source, a drain, a conductance between the source and drain that is controlled by the level of charge programmed onto a floating gate, and having a control gate and an erase electrode, a system for reading the state of an addressed cell by measuring the level of current passing therethrough, comprising:

means for passing current between the source and drain of the addressed cell in a manner to provide a current level between its source and drain that is proportional to the charge level programmed into the floating gate of the addressed cell,

at least two of said memory cells being provided as reference memory cells with charges programmed on their respective floating gates corresponding to respective at least two predetermined threshold levels, and

means connected to both of the addressed and reference memory cells for comparing the current flowing through the addressed cell with that flowing through said reference memory cells whereby the

programmed charge of said addressed cell is determined to lie within one of at least three regions demarcated by said predetermined thresholds, thereby to store at and read from the addressed cell more than one bit of information.

17. The system as in claim **16**, wherein the reading system is also part of a system for programming the memory cells in which each addressed cell is programmed to a desired state by altering the threshold incrementally by repetitive sequence of programming and reading to verify the state programmed until the desired state is reached.

18. The system as in claim **16**, wherein the reading system is also part of an erasing system in which each addressed cell is erased to the erased state by altering the threshold incrementally by repetitive sequence of erasing and reading to verify the state erased until the erased state is reached.

19. The memory array cell reading system according to claim **16**, wherein said comparing means includes a current mirror circuit connecting said addressed cell and said reference memory cells.

20. An EEprom memory system on an integrated circuit chip, comprising:

a plurality of groups of individually addressable EEprom cells,

a set of group reference EEprom cells associated with each group and constituted therefrom, thereby being electrically erasable with its associated group of cells and being programmable;

means responsive to signals from outside of said chip for programming said individually addressable EEprom cells to one of at least two conduction states,

means responsive to signals from outside of said chip for simultaneously erasing all the addressable and group reference EEprom cells of a designated group,

a set of master reference EEprom cells associated with said plurality of groups of individually addressable EEprom cells,

means responsive to signals from outside of said chip for erasing and programming a set of predetermined threshold levels into said set of master reference EEprom cells that correspond to breakpoints between said at least two conduction states,

reprogramming means after erasure of a designated group for duplicating the set of predetermined threshold levels from the set of master reference EEprom cells to the designated group's reference EEprom cells,

reading means responsive to signals from outside of said chip for comparing the threshold of an addressed individually addressable cell of a given group with the set of predetermined thresholds programmed into the set of group reference EEprom cells associated with said given group.

21. The system as in claim **20**, wherein the reading means is also part of a system for programming the memory cells in which each addressed cell is programmed to a desired state by altering the threshold incrementally by repetitive sequence of programming and reading to verify the state programmed until the desired state is reached.

22. The system as in claim **20**, wherein the reading means is also part of an erasing system in which each addressed cell is erased to the erased state by altering the threshold incrementally by repetitive sequence of erasing and reading to verify the state erased until the erased state is reached.

23. The system according to claim **20** wherein said set of master reference EEprom cells constitutes at least one EEprom cell for programming a reference predetermined threshold therein, and the set of predetermined thresholds is obtainable by scaling said reference predetermined threshold.

24. The memory system according to claim **20** wherein said reading means includes means for adjusting the master reference EEprom cells to correspond to the group reference EEprom cells, and means for comparing an addressed cell with the so adjusted master reference EEprom cells.

25. The system as in claim **24**, wherein the reading means is also part of a system for programming the memory cells in which each addressed cell is programmed to a desired state by altering the threshold incrementally by repetitive sequence of programming and reading to verify the state programmed until the desired state is reached.

26. The system as in claim **24**, wherein the reading means is also part of an erasing system in which each addressed cell is erased to the erased state by altering the threshold incrementally by repetitive sequence of erasing and reading to verify the state erased until the erased state is reached.

27. In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cell being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltage conditions for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, a system for programming data to EEprom cells including means for temporarily storing a chunk of data for programming a plurality of addressed cells, means for programming in parallel the stored chunk of data into the plurality of addressed cells, and means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data, wherein the improvement comprises:

means for inhibiting further programming of correctly verified cells among the plurality of addressed cells; and

means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly.

28. The system for programming the EEprom cells as in claim **27**, wherein the system resides on the EEprom integrated circuit chip.

29. In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cells being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltages for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing volt-

age conditions, a system residing on the EEprom integrated circuit chip for programming data to EEprom cells including means for temporarily storing a chunk of data for programming a plurality of addressed EEprom cells, means for programming in parallel the stored chunk of data into the plurality of addressed EEprom cells, and means for verifying the programmed data in each of the plurality of addressed EEprom cells with the chunk of stored data, wherein the improvement comprises:

means for inhibiting further programming of correctly verified cells among the plurality of addressed EEprom cells; and

means for further programming and verifying in parallel the plurality of addressed EEprom cells and inhibiting programming of correctly verified EEprom cells until all the plurality of addressed EEprom cells are verified correctly; and wherein

the verifying means includes a system for reading the stored charge of an addressed EEprom cell within ranges defined by one or more predetermined thresholds, said system for reading further comprising:

one or more reference memory EEprom cells that are each respectively programmed with a charge that substantially corresponds to each of said one or more predetermined thresholds; and

means responsive to said one or more reference EEprom cells for comparing the charge level of an addressed EEprom cell with that of said reference EEprom cells, thereby determining which of said plurality of said stored ranges that the addressed EEprom cell lies.

30. In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cells being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltages for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, a system residing on the EEprom integrated circuit chip for programing data to EEprom cells including means for temporarily storing a chunk of data for programming a plurality of addressed EEprom cells, means for programming in parallel the stored chunk of data into the plurality of addressed EEprom cells, and means for verifying the programmed data in each of the plurality of addressed EEprom cells with the chunk of stored data, wherein the improvement comprises:

means for inhibiting further programming of correctly verified cells among the plurality of addressed EEprom cells; and

means for enabling further programming and verifying in parallel the addressed EEprom cells and inhibiting programming of correctly verified cells until all the plurality of addressed EEprom cells are verified correctly; and wherein

the array of EEprom cells are grouped such that all cells in each group are erasable simultaneously; and wherein

the verifying means includes a reading circuit further comprising:

one or more sets of group reference EEprom cells, each set being constituted from a group of EEprom cells associated therewith, thereby being electrically erasable with its associated group of cells and being programmable,

means responsive to signals from outside of said chip for programming said individually addressable EEprom cells to one of at least two conduction states,

means responsive to signals from outside of said chip for simultaneously erasing all the addressable and reference EEprom cells of a designated group,

a set of master reference EEprom cells constituted from EEprom cells of the plurality of groups of individually addressable EEprom cells,

means responsive to signals from outside of said chip for erasing and programming a set of predetermined threshold levels into said set of master reference EEprom cells that correspond to breakpoints between said at least two conduction states,

reprogramming means after erasure of a designated group for duplicating the set of predetermined thresholds from the set of master reference EEprom cells to the designated group's reference EEprom cells,

reading means for comparing the threshold of an addressed individually addressable cell of a given group with the set of predetermined thresholds programmed into the set of group reference EEprom cells associated with said given group.

31. The memory system according to claim **30** wherein said reading means includes means for adjusting the master reference EEprom cells to correspond to the group reference EEprom cells, and means for comparing an addressed cell with the so adjusted master reference EEprom cells.

32. In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cells being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltages for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, a system residing on the EEprom integrated circuit chip for programming data to EEprom cells including means for temporarily storing a chunk of data for programming a plurality of addressed cells, means for programming in parallel the stored chunk of data into the plurality of addressed cells, and means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data, wherein the improvement comprises:

means for enabling further programming and verifying in parallel to one or more of the addressed cells until all the plurality of addressed cells are verified; and

means on chip for individually inhibiting programming of any addressed cell already verified, while enabling further programming in parallel to all other addressed cells not yet verified.

33. The system according to claim **32**, wherein the memory cells have more than two states.

34. The system according to claim **32**, wherein the memory cells have binary states.

35. In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cell being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltages for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, a system for erasing the EEprom cells including means for erasing in parallel a plurality of addressed EEprom cells, means for verifying the memory state in each of the plurality of addressed EEprom cells, means for enabling further erasing in parallel to one or more of the addressed EEprom cells until all the plurality of addressed EEprom cells are verified to be in an erased state, said verifying means includes a system for reading the stored charge of an addressed cell within ranges defined by one or more predetermined threshold levels, wherein the improvement in said system for reading comprising:

one or more reference memory cells that are each respectively programmed with a charge that is substantially equal to or proportional to each of said one or more thresholds; and

means responsive to said one or more reference EEprom cells for comparing the charge level of an addressed cell with that of said reference EEprom cells, thereby determining in which of said plurality of said stored ranges the addressed cell lies.

36. The system for erasing the EEprom cells as in claim 35, wherein the system resides outside the EEprom integrated circuit chip.

37. The system for erasing the EEprom cells as in claim 35, wherein the system resides on the EEprom integrated circuit chip.

38. In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cell being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltages for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, the memory cells are grouped such that all cells in the group are erasable simultaneously, a system for erasing the EEprom cells including means for erasing in parallel a plurality of addressed EEprom cells, means for verifying the memory state in each of the plurality of addressed EEprom cells, means for enabling further erasing in parallel to one or more of the addressed EEprom cells until all the plurality of addressed EEprom cells are verified to be in an erased state, said verifying means includes a reading circuit for reading the stored charge of an addressed cell within ranges defined by one or more predetermined threshold levels, wherein the improvement in said system for reading comprises:

one or more group reference EEprom cells provided as part of each of said group of memory cells,

means for programming said individually addressable EEprom cells to one of at least two conduction states,

means for simultaneously erasing all the addressable and reference EEprom cells of a designated group,

one or more master reference EEprom cells,

means for erasing and programming different threshold levels on each of said one or more master reference EEprom cells that correspond to breakpoints between said at least two conduction states,

means responsive to said individually addressable EEprom cells of a group being programmed for programming that group's reference EEprom cells to the levels of said master reference EEprom cells,

means for reading an addressed individually addressable cell of a given group of cells by comparison with the reference EEprom cells of said given group.

39. The memory system according to claim 38 wherein said reading means includes means for adjusting the master reference EEprom cells to correspond to the group reference EEprom cells, and means for comparing an addressed cell with the so adjusted master reference EEprom cells.

40. In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cell being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltages for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications or programming or erasing voltage conditions, a system for erasing the EEprom cells including means for erasing in parallel a plurality of addressed EEprom cells, means for verifying the memory state in each of the plurality of addressed EEprom cells means for enabling further erasing in parallel to one or more of the addressed EEprom cells until all the plurality of addressed EEprom cells are verified to be in an erased state; wherein the improvement in the system for programming comprises:

means on chip for individually inhibiting erasing of any addressed cell already verified, while enabling further erasing in parallel to all other addressed cells not yet verified.

41. The system according to claim 40, wherein the memory cells have more than two states.

42. The system according to claim 40, wherein the memory cells have binary states.

43. In an array of addressable semiconductor electrically erasable and programmable memory cells on an integrated circuit chip, the memory cell being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltage conditions for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, a system for erasing the EEprom memory cells including means for erasing in parallel a plurality of addressed cells, means for verifying the memory state in each of the plurality of addressed cells, means for enabling further erasing in parallel to one or more of the addressed cells until all the plurality of addressed cells are verified to be in an erased state, wherein the improvement comprises:

means for programming the cells in the erased state to the memory state adjacent the erased state, thereby ensuring uniformity of threshold level in each of the erased cells and that each cell is subject to similar amount of program/erase cycling.

44. In a EEprom system including an array of addressable semiconductor electrically erasable and programmable memory cells on an integrated circuit chip, a controller for controlling the operation of the memory cells, means for temporarily storing on chip a chunk of data transferred from the controller, means for programming in parallel the stored chunk of data into the plurality of addressed cells, means for verifying on chip the programmed data in each of the plurality of addressed cells with the chunk of stored data, means for enabling further programming in parallel to one or more of the addressed cells until all the plurality of addressed cells are verified, wherein the improvement in programming the plurality of addressed memory cells comprises:

means on chip for individually inhibiting programming of any addressed memory cell already verified, while enabling further programming in parallel of all other addressed memory cells not yet verified.

45. In an integrated circuit memory system having an array of a plurality of addressable semiconductor electrically erasable and programmable memory (EEprom) cells of the type having a source, a drain, a control gate, a floating gate capable of retaining a charge level programmed into it during use of the memory system, resulting in a definite memory state having a corresponding threshold of conduction relative to one or more predetermined threshold levels used to demarcate memory states, and an erase electrode capable of removing charge from said floating gate, and said memory system including a reading system for determining the programmed state of an addressed cell, said reading system comprising:

one or more reference memory cells constituted from the array of EEprom cells that are each respectively programmed with a charge that corresponds to each of said one or more predetermined thresholds; and

means responsive to said one or more reference memory cells for comparing the charge level of an addressed cell with that of said one or more reference memory cells, thereby determining relative to which of said one or more predetermined threshold levels the addressed cell lies, whereby one or more bits of data stored in the addressed cell is readable therefrom.

46. The memory cell reading system according to claim **45**, which additionally includes means for independently erasing and programming said one or more reference memory cells to said one or more predetermined thresholds from outside of said memory.

47. The memory cell reading system according to claim **45**, wherein said one or more reference memory cells constitute at least one cell for programming a reference predetermined threshold therein, and said one or more predetermined thresholds are obtainable by scaling said reference predetermined threshold.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,172,338
DATED : December 15, 1992
INVENTOR(S) : Sanjay Mehrotra; Eliyahou Harari

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

ON THE TITLE PAGE:

Delete Winston Lee as a named inventor.

Signed and Sealed this

Second Day of November, 1993

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : B1 5,172,338
DATED : July 8, 1997
INVENTOR(S) : Sanjay Mehrotra et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 1, Line 37, in Claim 32 replace:
"of programming of erasing voltage conditions, a system" with

--of programming or erasing voltage conditions, a system

In Column 2, Line 45-46 in Claim 55 replace:
"to specific memory states include at least separated break-point threshold levels and further including means for" with

--to specific memory states include at least two separated break-point threshold levels, and further including means for--

Signed and Sealed this

Twenty-eighth Day of July, 1998

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

US005172338B1

REEXAMINATION CERTIFICATE (3256th)

United States Patent [19] [11] B1 5,172,338

Mehrotra et al. [45] Certificate Issued Jul. 8, 1997

[54] **MULTI-STATE EEPROM READ AND WRITE CIRCUITS AND TECHNIQUES**

[75] Inventors: **Sanjay Mehrotra**, Milpitas; **Eliyahou Harari**, Los Gatos; **Winston Lee**, San Francisco, all of Calif.

[73] Assignee: **Sandisk Corporation**, Santa Clara, Calif.

Reexamination Requests:
No. 90/004,352, Sep. 6, 1996
No. 90/004,387, Sep. 27, 1996

Reexamination Certificate for:

Patent No.:	**5,172,338**
Issued:	**Dec. 15, 1992**
Appl. No.:	**508,273**
Filed:	**Apr. 11, 1990**

Certificate of Correction issued Nov. 2, 1993.

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 337,579, Apr. 13, 1989.

[51] **Int. Cl.**[6] **G11C 7/00**; G11C 29/00; G11C 16/04

[52] **U.S. Cl.** **365/185.03**; 365/184; 365/185.33; 365/189.07; 365/195; 365/201

[58] **Field of Search** 365/185.03, 184, 365/185.33, 189.07, 195, 201

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,090,258	5/1978	Cricchi	365/184
4,149,270	4/1979	Cricchi et al.	365/222
4,279,024	7/1981	Schrenk	365/185.22
4,357,685	11/1982	Danielle et al.	365/185.22
4,393,475	7/1983	Kitagawa et al.	365/201
4,415,992	11/1983	Adlhoch	365/94
4,495,602	1/1985	Sheppard	365/104
4,599,707	7/1986	Fang	365/185.02
4,718,041	1/1988	Baglee et al.	365/185.22
4,763,305	8/1988	Kuo	365/185.22
4,805,151	2/1989	Terada et al.	365/185.13
4,807,188	2/1989	Casagrande	365/182
4,811,294	3/1989	Kobayashi et al.	365/185.22
4,956,816	9/1990	Atsumi et al.	365/201
4,999,813	3/1991	Ohtsuka et al.	365/201
5,053,990	10/1991	Kreifels et al.	365/185.02
5,095,344	3/1992	Harari .	

FOREIGN PATENT DOCUMENTS

59-31158	7/1984	Japan .
62-257699	5/1987	Japan .
2061651	5/1981	United Kingdom .

OTHER PUBLICATIONS

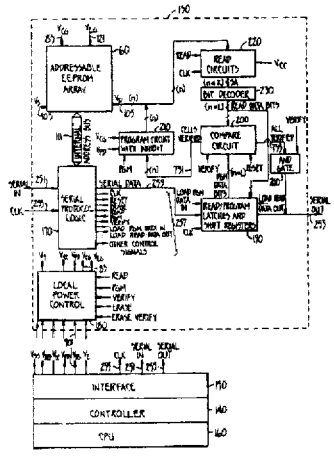
Krick, P.J., "Three–State MNOS Fet Memory Array," *IBM Technical Disclosure Bulletin*, vol. 18, No. 12, pp. 4192–4193 (May 1976).

(List continued on next page.)

Primary Examiner—A. Zarabian

[57] **ABSTRACT**

Improvements in the circuits and techniques for read, write and erase of EEprom memory enable non-volatile multi-state memory to operate with enhanced performance over an extended period of time. In the improved circuits for normal read, and read between write or erase for verification, the reading is made relative to a set of threshold levels as provided by a corresponding set of reference cells which closely track and make adjustment for the variations presented by the memory cells. In one embodiment, each Flash sector of memory cells has its own reference cells for reading the cells in the sector, and a set of reference cells also exists for the whole memory chip acting as a master reference. In another embodiment, the reading is made relative to a set of threshold levels simultaneously by means of a one-to-many current mirror circuit. In improved write or erase circuits, verification of the written or erased data is done in parallel on a group of memory cells at a time and a circuit selectively inhibits further write or erase to those cells which have been correctly verified. Other improvements includes programming the ground state after erase, independent and variable power supply for the control gate of EEprom memory cells.



OTHER PUBLICATIONS

Alberts, et al., "Multi-Bit Storage Fet EAROM Cell," *IBM Technical Disclosure Bulletin,* vol. 24, No. 7A, pp. 3311-3314 (Dec. 1981).

Bleiker, et al., "A Four-State EEPROM Using Floating-Gate Memory Cells," *IEEE Journal of Solid-State Circuits,* SC-22 (1987) Jun., No. 3, New York, NY, USA.

Torelli et al., "An improved method for programming a word-erasable EEPROM," *Alta Frequenza,* vol. LII, No. 6, pp. 487-494, Nov.-Dec. 1983.

Torelli et al., "Single Chip, 16-Station TV Digital Tuning System," *SGS-ATES Technical* Note 170, pp. 1-19 (1984).

Torelli et al., "PLL2K-PLL Frequency Synthesizer For 30 Programs," *SGS-ATES Componenti Electronici SpA,* Technical Note 152, pp. 1-16 (1982).

Scrocchi et al., "EPM32-Electronic Program Memory System For TV (32 Stations)," *SGS-ATES Componenti Electronici SpA,* Technical Note 153, pp. 1-19 (1982).

"EPM 16-Electronic Program Memory (16 Stations)," *SGS-ATES Componenti Electronici SpA,* MOS Integrated Circuits/M193A-M193C-M193D, 15 pps, (Nov., 1981).

"EPM-32 Electronic Program Memory (32 Stations)," *SGS-ATES Componenti Electronici SpA,* MOS Integrated Circuits/M293, 16 pps. (Oct., 1982).

"Single Chip Non-Volatile Station Memory, PCM Remote Control Receiver and Display Driver," *SGS-ATES Componenti Electronici SpA,* MOS Integrated Circuits/M490-M491, 24 pps. (May, 1983).

"PLL TV Mircocomputer Interface," *SGS-ATES Componenti Electronici SpA,* MOS Integrated Circuits/M290, 15 pps. (Jun. 1982).

Gee et al., "An Enhanced 16K E^2PROM," *IEEE Journal of Solid State Circuits,* vol. SC-17, No. 5 (Oct. 1982).

Torelli, "An LSI technology fully compatible EAROM cell," *S-ATES Componenti Elettronici SpA,* 7pp (1982).

Caironi et al., "A TV Frequency Synthesis System With A Single Chip Microprocessor Interface Including Non Volatile Memory," *IEEE Transactions on Consumer Electronics,* vol. CE-28, No. 3, pp. 363-371 (Aug. 1982).

Torelli et al., "Integrating Non-Volatile Station Memory and Remote Control Receiver In A Single Chip," *IEEE Digest of Technical Papers,* Cat. No. 83CH1872-1, 2pp. (Jun. 1983).

Torelli et al., "Non-Volatile Station Memory Single Chip Including Remote Control Receiver and Memory Display Driver," *IEEE Transactions on Consumer Electronics,* vol. CE-29, No. 3, pp. 103-113 (Aug. 1983.

Excerpts from a 1983 Data Book published by SGS-Ates Group, 45 pp. (Nov. 1983).

Berenga et al., "E^2-PROM TV Synthesizer," *IEEE Digest of Technical Papers,* Cat. No. 78CH1298-9SSC, 4 pp. (Feb. 1978).

Klingman, "Microprocessor Systems Digest," *Prentice-Hall, Inc.,* pp. 30-31 (1977).

Masuoka et al., "A 256-kbit Flash E^2PROM Using Triple-Polysilicon Technology," *IEEE Journal of Solid-State Circuits,* vol. SC-22, No. 4, (Aug. 1987).

REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **1–31**, **35–43** and **45–47** is confirmed.

Claims **32** and **44** are determined to be patentable as amended.

Claims **33** and **34**, dependent on an amended claim, are determined to be patentable.

New claims **48–65** are added and determined to be patentable.

32. In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cells being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltages for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming of erasing voltage conditions, a system residing on the EEprom integrated circuit chip for programming data to EEprom cells including means for temporarily storing a chunk of data for programming a plurality of addressed cells, means for programming in parallel the stored chunk of data into the plurality of addressed cells, and means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data, wherein the improvement comprises:

means for enabling further programming and verifying in parallel to one or more of the addressed cells until all the plurality of addressed cells are verified; and

means on chip for individually inhibiting programming of any addressed cell already verified *until all the addressed cells are verified*, while enabling further programming in parallel to all other addressed cells not yet verified.

44. In a EEprom system including an array of addressable semiconductor electrically erasable and programmable memory cells on an integrated circuit chip, a controller for controlling the operation of the memory cells, means for temporarily storing on chip a chunk of data transferred from the controller, means for programming in parallel the stored chunk of data into the plurality of addressed cells, means for verifying on chip the programmed data in each of the plurality of addressed cells with the chunk of stored data, means for enabling further programming in parallel to one or more of the addressed cells until all the plurality of addressed cells are verified, wherein the improvement in programming the plurality of addressed memory cells comprises:

means on chip for individually inhibiting programming of any addressed memory cell already verified *until all the addressed cells are verified*, while enabling further programming in parallel of all other addressed memory cells not yet verified.

48. The system for programming the EEprom cells as in either of claims 27 or 28, wherein said means for inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly includes a plurality of latches and means for setting individual ones of the latches in response to corresponding ones of said plurality of addressed cells being verified.

49. The system for programming the EEprom cells as in claim 48, wherein said means for verifying the programmed data includes means for detecting a parameter related to the charge levels of the individual programmed cells, and means for comparing the parameter detected from the individual programmed cells with at least one reference parameter related to corresponding individual bits of the chunk of data being programmed, wherein individual programmed cells are verified upon said comparison of parameters being achieved.

50. The system for programming the EEprom cells as in any one of claims 27, 28 or 44, wherein the memory cells individually have more than two specific states.

51. The system for programming the EEprom cells as in any one of claims 27, 28 or 44, wherein the memory cells individually have exactly two specific states.

52. The system for programming the EEprom cells as in either of claims 27 or 28, wherein specific charge levels corresponding to specific memory states include at least one breakpoint threshold level, and wherein the verifying means includes means for reading the states of the memory cells by programming into the specific memory states by a margin.

53. The system for programming the EEprom cells as in claim 52 wherein said specific charge levels corresponding to a specific memory state include exactly one breakpoint threshold level.

54. The system for programming the EEprom cells as in claim 52 wherein said specific charge levels corresponding to specific memory states include more than one breakpoint threshold level.

55. The system for programming the EEprom cells as in claim 52, wherein said specific charge levels corresponding to specific memory states include at least separated breakpoint threshold levels and further including means for programming the memory cells with successive applications of voltages that individually shift the threshold by less than one half of a difference between said at least two separated breakpoint threshold levels.

56. The system according to any one of claims 27, 28, 32-34 and 44, wherein said verifying means includes means for comparing the programmed data in each of the plurality of addressed cells with the chunk of stored data.

57. The system for programming the EEprom cells as in either of claims 27 or 28, further including means for programming the memory cells with successive applications of voltages such that a plurality of said applications are required to change from one specific state of the cell to another.

58. The system for programming the EEprom cells as in any one of claims 27, 28, or 32-34, wherein the memory cell erase electrode includes an erase gate.

59. The system for programming the EEprom cells as in either of claims 27 or 28, wherein at least one reference cell is included in individual ones of the blocks of cells, and which additionally comprises means for programming said

at least one reference cell to a reference level, and wherein said verifying means includes means for reading the reference level of the reference cell of the block wherein the plurality of addressed cells reside to verify the programmed data.

60. The system for programming the EEprom cells as in either of claims 27 or 28, which includes a reference memory cell, and which additionally comprises means for programming said reference cell to a reference level, and wherein said verifying means includes means for reading the reference level of said at least one reference cell for verifying the programmed data.

61. The system for programming the EEprom cells as in either of claims 27 or 28, wherein the array of memory cells includes a plurality of conductive bit lines having the sources and drains of individual ones of said memory cells respectively connected to adjacent ones of said bit lines, and a plurality of conductive word lines that individually connect to the control gates of a plurality of adjacent memory cells.

62. The system for programming the EEprom cells as in claim 61 wherein the individual memory cells include a select transistor.

63. The system for programming the EEprom cells as in either of claims 27 or 28, which additionally includes means operable after application of erase voltages to the addressed at least one block for adjusting to an erased charge level any cells of said at least one block that were overerased.

64. The system for programming the EEprom cells as in either of claims 27 or 28, wherein the array of addressable memory cells is organized into a plurality of addressable blocks characterized by the cells of an individual block being erasable together, and which further comprises means for simultaneously applying erase voltages to the memory cells within individual addressed ones of said plurality of addressable blocks.

65. The system for programming the EEprom cells as in claim 64, wherein said erase means includes means connectable to individual addressed ones of said plurality of addressable blocks for simultaneously applying erase voltages to memory cells therewithin that are in at least first and second different specific memory states before application of erase voltages thereto.

* * * * *

EXHIBIT J

US005991517A

United States Patent [19]

Harari et al.

[11] **Patent Number: 5,991,517**

[45] **Date of Patent: *Nov. 23, 1999**

[54] **FLASH EEPROM SYSTEM WITH CELL BY CELL PROGRAMMING VERIFICATION**

[75] Inventors: **Eliyahou Harari**, Los Gatos; **Robert D. Norman**, San Jose; **Sanjay Mehrotra**, Milpitas, all of Calif.

[73] Assignee: **SanDisk Corporation**, Sunnyvale, Calif.

[*] Notice: This patent is subject to a terminal disclaimer.

[21] Appl. No.: **08/771,708**

[22] Filed: **Dec. 20, 1996**

Related U.S. Application Data

[63] Continuation of application No. 08/174,768, Dec. 29, 1993, Pat. No. 5,602,987, which is a continuation of application No. 07/963,838, Oct. 20, 1992, Pat. No. 5,297,148, which is a division of application No. 07/337,566, Apr. 13, 1989, abandoned.

[51] **Int. Cl.**[6] **G06F 11/00**

[52] **U.S. Cl.** **395/182.01**; 395/182.06

[58] **Field of Search** 365/185.22, 185.19, 365/189.01, 226, 201; 395/182.06, 182.01

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,090,258	5/1978	Cricchi	365/184
4,149,270	4/1979	Cricchi et al.	365/222

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

5931158	of 1984	Japan .
62257699	of 1987	Japan .
2061651	of 1981	United Kingdom .

OTHER PUBLICATIONS

Torelli et al., "An improved method for programming a word–erasable EEprom," *Alta Frequenza,* vol. LII, No. 6, pp. 487–494, Nov.–Dec. 1983.

Torelli et al., "Single Chip, 16–Station TV Digital Tuning System," *SGS–ATES* Technical Note 170, pp. 1–19 (1984).

Torelli et al., "PLL2K–PLL Frequency Synthesizer For 30 Programs," *SGS–ATES Componenti Electronici SpA,* Technical Note 152, pp. 1–16 (1982).

Scroochi et al., "EPM32–Electronic Program Memory System For TV (32 Stations)," *SGS–ATES Componenti Electronici SpA,* Technical Note 153, pp. 1–19 (1982).

"EPM 16–Electronic Program Memory (16 Stations)," *SGS–ATES Componenti Electronici SpA,* MOS Integrated Circuits/M193A–M193C–M193D, 15 pps, (Nov., 1981).

"EPM–32 Electronic Program Memory (32 Stations)," *SGS–ATES Componenti Electronici SpA,* Mos Integrated Circuits/M293, 16 pps. (Oct., 1982).

(List continued on next page.)

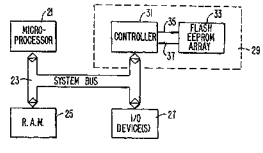
Primary Examiner—Ly Hua

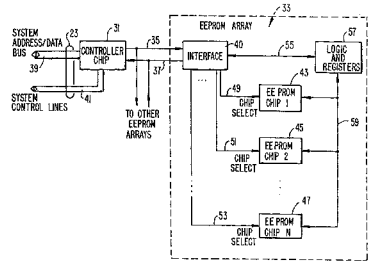
Attorney, Agent, or Firm—Majestic, Parsons, Siebert & Hsue

[57] **ABSTRACT**

A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement individually verifies the states of a plurality of cells that are being programmed in parallel in order to terminate the programming, as a result of the verification, on a cell-by-cell basis as the cells reach their programmed states.

39 Claims, 22 Drawing Sheets





U.S. PATENT DOCUMENTS

4,181,980	1/1980	McCoy	365/185.45
4,253,059	2/1981	Bell et al.	371/21.4
4,272,830	6/1981	Moench	365/45
4,279,024	7/1981	Schrenk	365/185.22
4,287,570	9/1981	Stark	365/104
4,357,685	11/1982	Daniels et al.	365/185.22
4,393,475	7/1983	Kitagawa et al.	365/185.21
4,415,992	11/1983	Adlhoch	365/94
4,460,982	7/1984	Gee et al.	365/185.19
4,495,602	1/1985	Sheppard	365/104
4,586,163	4/1986	Koike	365/104
4,599,707	7/1986	Fang	35/185.02
4,612,629	9/1986	Harari	365/185.08
4,653,023	3/1987	Suzuki et al.	365/104
4,718,041	1/1988	Baglee et al.	365/185.22
4,733,394	3/1988	Giebel	371/21
4,752,929	6/1988	Kantz et al.	371/21.2
4,763,305	8/1988	Kuo	365/185.22
4,779,272	10/1988	Kohda et al.	365/185.2
4,799,195	1/1989	Iwahashi et al.	365/185.21
4,805,151	2/1989	Terada et al.	371/21.1
4,807,188	2/1989	Casagrande	3655/185.05
4,809,231	2/1989	Shannon et al.	365/201
4,811,294	3/1989	Kobayashi et al.	365/185.22
4,847,808	7/1989	Kobatake	365/104
4,870,618	9/1989	Iwashita	365/185.18
4,956,816	9/1990	Atsumi et al.	365/185.22
4,999,813	3/1991	Ohtsuka et al.	365/185.18
5,003,510	3/1991	Hamisaki	365/189.01
5,053,990	10/1991	Kreifels et al.	711/103
5,095,344	3/1992	Harari et al.	357/23.5
5,163,021	11/1992	Mehrotra et al.	365/185
5,172,338	12/1992	Mehrotra et al.	365/185
5,297,148	3/1994	Harari et al.	371/10.2
5,602,987	2/1997	Harari et al.	395/182.06

OTHER PUBLICATIONS

"Single Chip Non–Volatile Station Memory, PCM Remote Control Receiver and Display Driver," *SGS–ATES Componenti Electronici SpA,* MOS Integrated Circuits/M490–M491, 24 pps. (May, 1983).

"PLL TV Microcomputer Interface," *SGS–ATES Componenti Electronici SpA,* MOS Integrated Circuits/M290, 15 pps. (Jun., 1982).

Gee et al., "An Enhanced 16K E^2PROM," *IEEE Journal of Solid State Circuits,* vol. SC–17, No. 5 (Oct. 1982).

Torelli, "An LSI technology fully compatible EAROM cell," *SGS–ATES Componenti Electronici SpA,* 7pp. (1982).

Caironi et al., "A TV Frequency Synthesis System With A Single Chip Microprocessor Interface Including Non Volatile Memory," *IEEE Transactions on Consumer Electronics,* vol. CE–28, No. 3, pp. 363–371 (Aug. 1982).

Torelli et al., "Integrating Non–Volatile Station Memory and Remote Control Receiver In A Single Chip," *IEEE Digest of Technical Papers,* Cat. No. 83CH1872–1, 2pp. (Jun., 1983).

Torelli et al., "Non–Volatile Station Memory Single Chip Including Remote Control Receiver and Memory Display Driver," *IEEE Transactions on Consumer Electronics,* vol. CE–29, No. 3, pp. 103–113 (Aug. 1983).

Excerpts from a 1983 Data Book published by SGS–ATES Group, 45 pp. (Nov. 1983).

Berenga et al., "E^2–PROM TV Synthesizer," *IEEE Digest of Technical Papers,* Cat. No. 78CH1298–9SSC, 4 pp. (Feb. 1978).

Klingman, "Microprocessor Systems Design," *Prentice–Hall, Inc.,* pp. 30–31 (1977).

Masuoka et al., "A 256–kbit Flash E^2PROM Using Triple–Polysilicon Technology," *IEEE Journal of Solid–State Circuits,* vol. SC–22, No. 4, (Aug. 1987).

Bleiker et al., "A Four–State EEPROM Using Floating–Gate Memory Cells," *IEEE Journal of Solid–State Circuits,* vol. SC–22, No. 3 (Jun., 1987).

Krick, P.J., "Three–State MNOS Fet Memory Array," *IBM Technical Disclosure Bulletin,* vol. 18, No. 12, pp. 4192–4193 (May, 1976).

Alberts, et al., "Multi–Bit Storage Fet EAROM Cell," *IBM Technical Disclosure Bulletin,* vol. 24, No. 7A, pp. 3311–3314 (Dec. 1981).

Stark, M., "Two Bits Per Cell Rom," *IEEE Catalog No. 81–CH1626–1,* Library of Congress No. 80–85186, Order No. 341, Spring Comp Con 1981, Feb. 23–26, Twenty–Second Computer Society International Conference, San Francisco, CA.

Furuyama et al., "An Experimental 2–Bit/Cell Storage Dram For Macro Cell or Memory–On–Logic Application," pp. 4.4.1–4.4.4, *IEEE,* (1988).

Horiguchi et al., "An Experimental Large–Capacity Semiconductor File Memory Using 16–Levels Cell Storage," *IEEE Journal Of Solid–State Circuits,* vol. 23, No. 1, Feb. 1988.

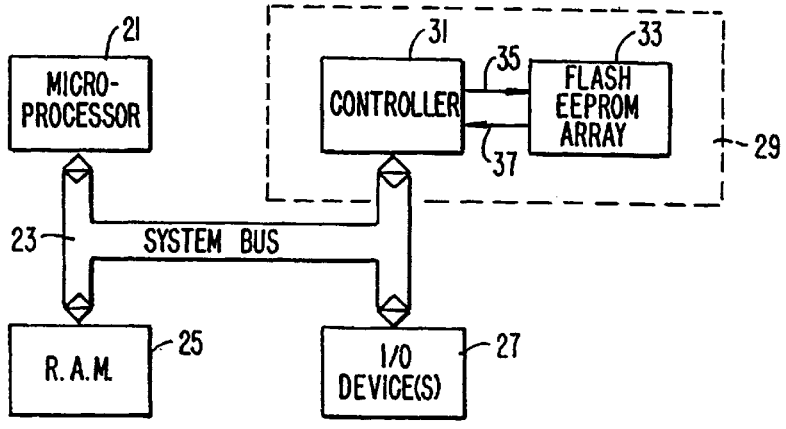

21
MICRO-PROCESSOR
31
CONTROLLER
35
33
FLASH EEPROM ARRAY
37
29
23
SYSTEM BUS
R.A.M.
25
I/O DEVICE(S)
27

FIG._1A

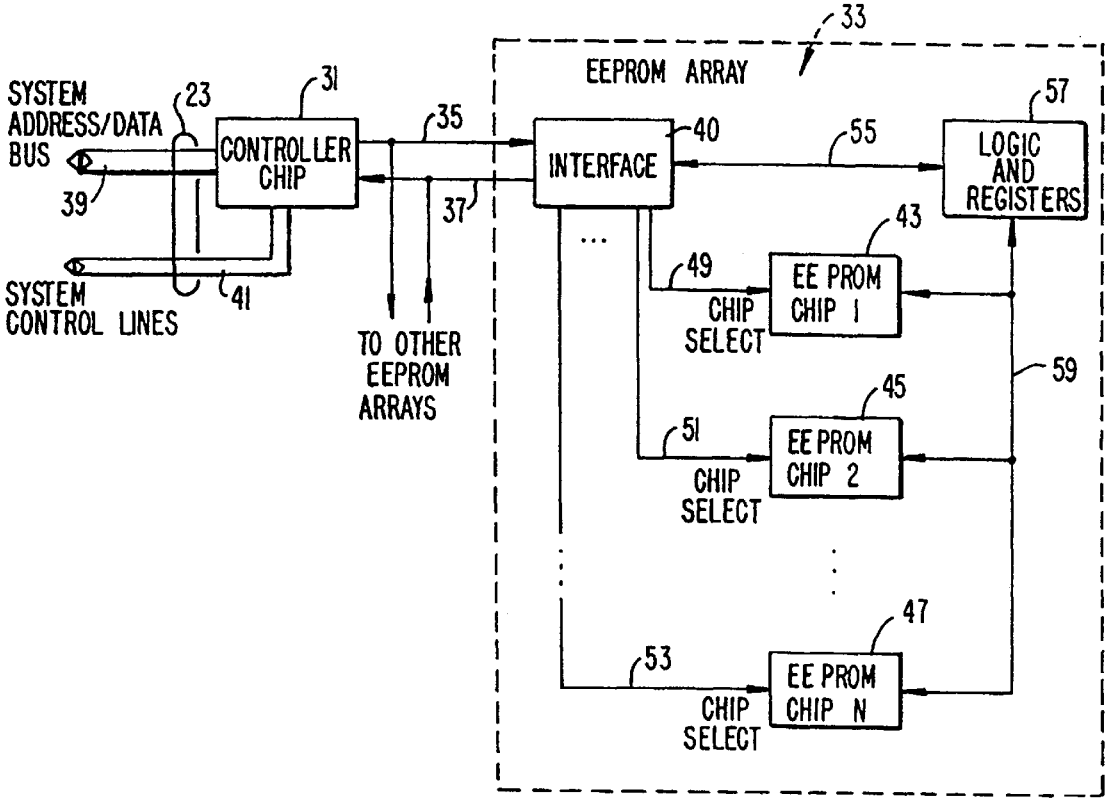

33
EEPROM ARRAY
SYSTEM ADDRESS/DATA BUS
23
31
CONTROLLER CHIP
35
39
37
SYSTEM CONTROL LINES
41
TO OTHER EEPROM ARRAYS
INTERFACE
40
55
57
LOGIC AND REGISTERS
43
49
CHIP SELECT
EE PROM CHIP 1
59
45
51
CHIP SELECT
EE PROM CHIP 2
47
53
CHIP SELECT
EE PROM CHIP N

FIG._1B

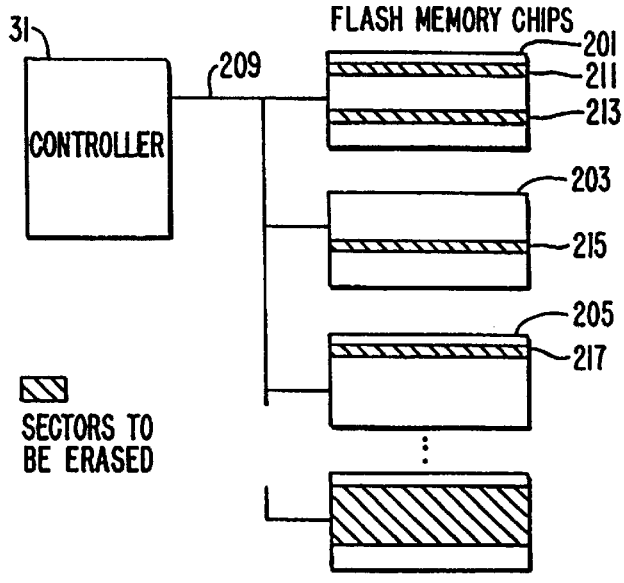


FIG._2

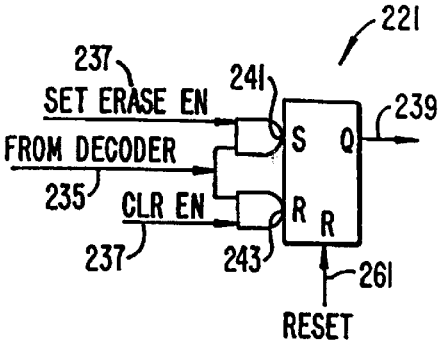


FIG._3B

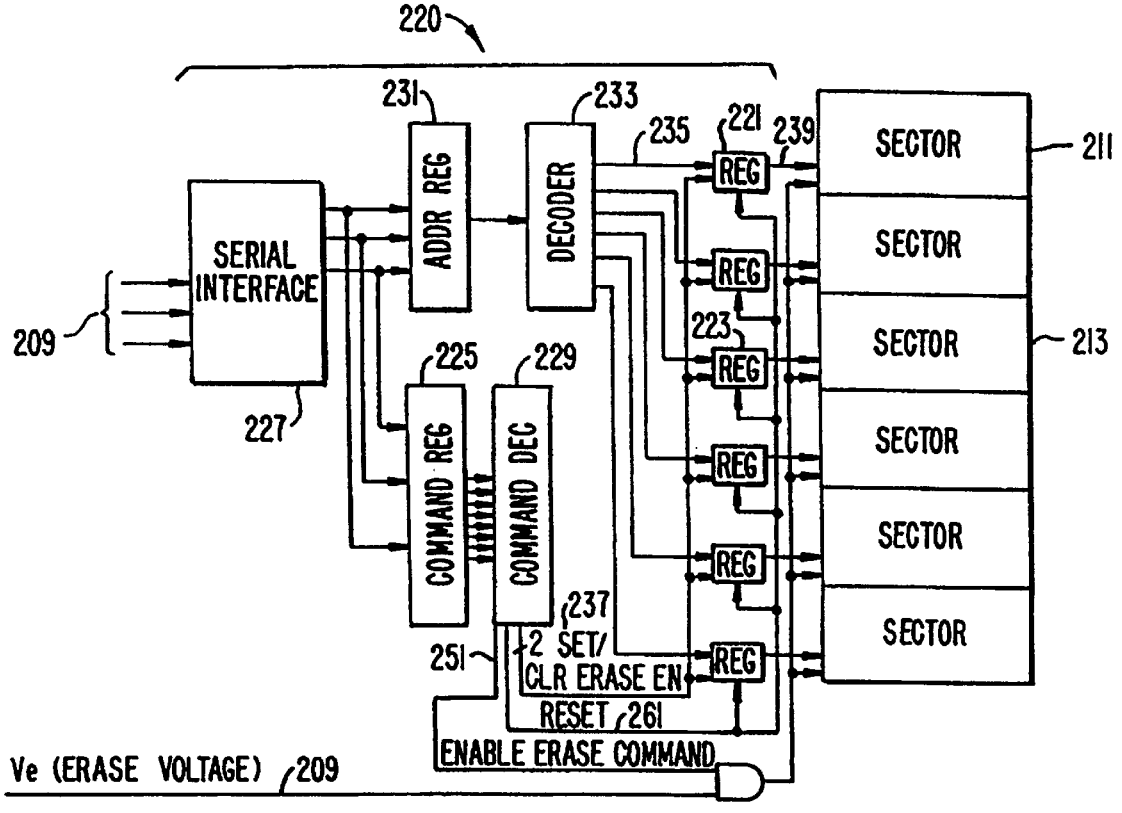


FIG._3A

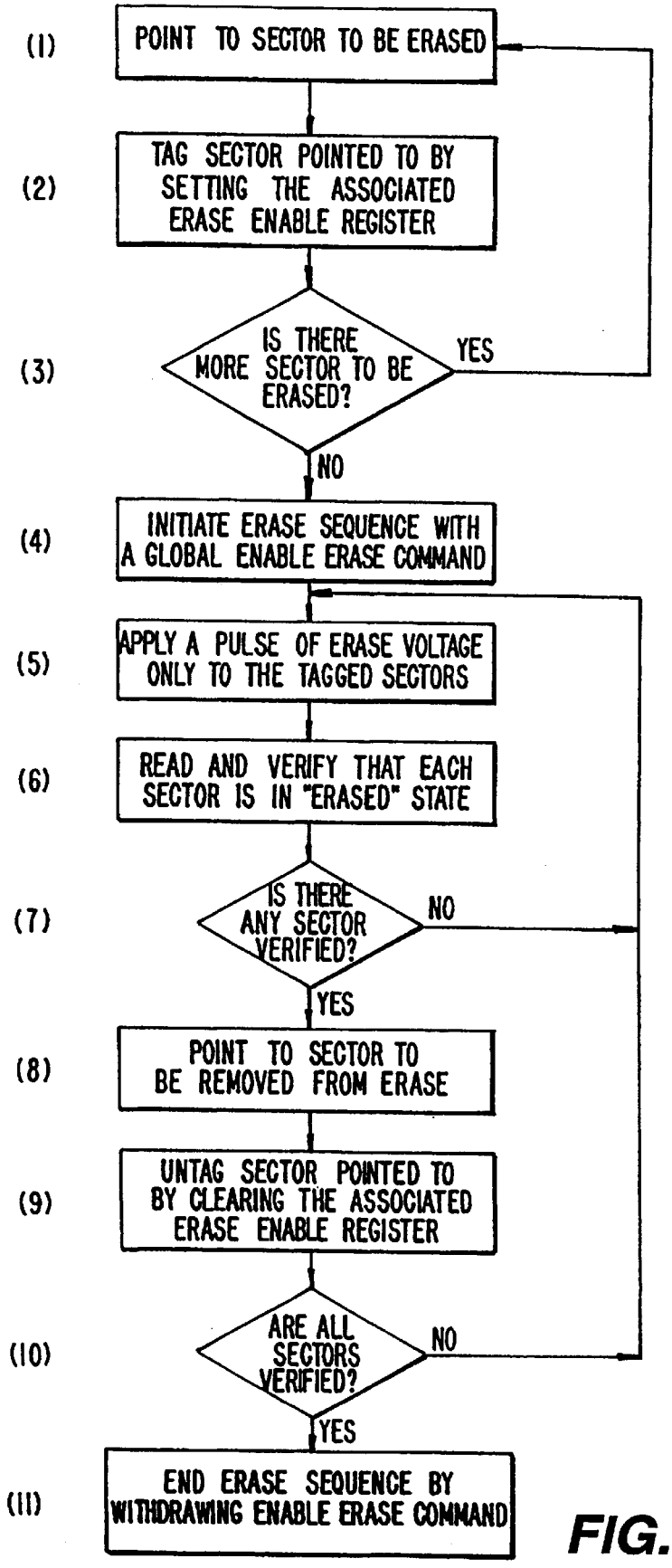

(1)
POINT TO SECTOR TO BE ERASED
(2)
TAG SECTOR POINTED TO BY SETTING THE ASSOCIATED ERASE ENABLE REGISTER
(3)
IS THERE MORE SECTOR TO BE ERASED?
YES
NO
(4)
INITIATE ERASE SEQUENCE WITH A GLOBAL ENABLE ERASE COMMAND
(5)
APPLY A PULSE OF ERASE VOLTAGE ONLY TO THE TAGGED SECTORS
(6)
READ AND VERIFY THAT EACH SECTOR IS IN "ERASED" STATE
(7)
IS THERE ANY SECTOR VERIFIED?
NO
YES
(8)
POINT TO SECTOR TO BE REMOVED FROM ERASE
(9)
UNTAG SECTOR POINTED TO BY CLEARING THE ASSOCIATED ERASE ENABLE REGISTER
(10)
ARE ALL SECTORS VERIFIED?
NO
YES
(11)
END ERASE SEQUENCE BY WITHDRAWING ENABLE ERASE COMMAND

FIG._4

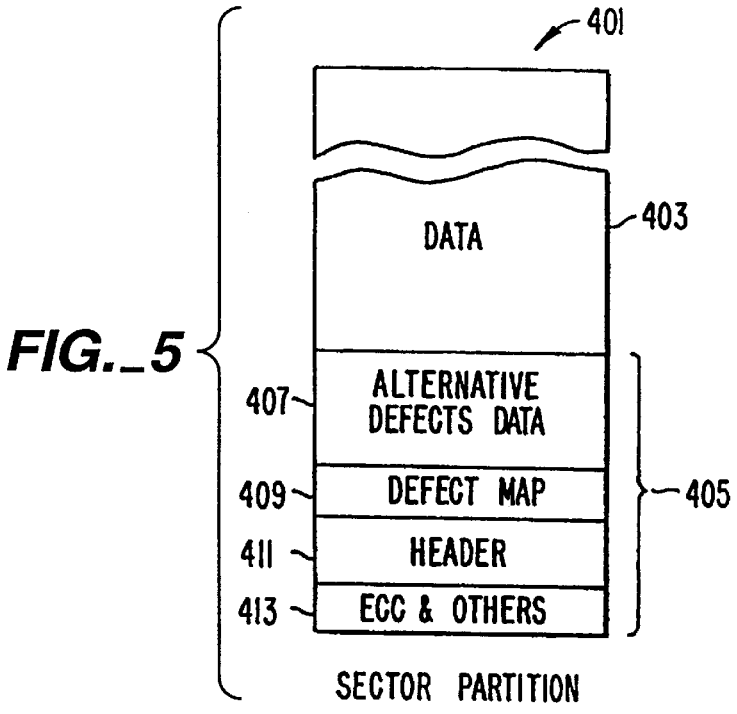

401
DATA
403
ALTERNATIVE DEFECTS DATA
407
DEFECT MAP
409
HEADER
411
ECC & OTHERS
413
405
SECTOR PARTITION

FIG._5

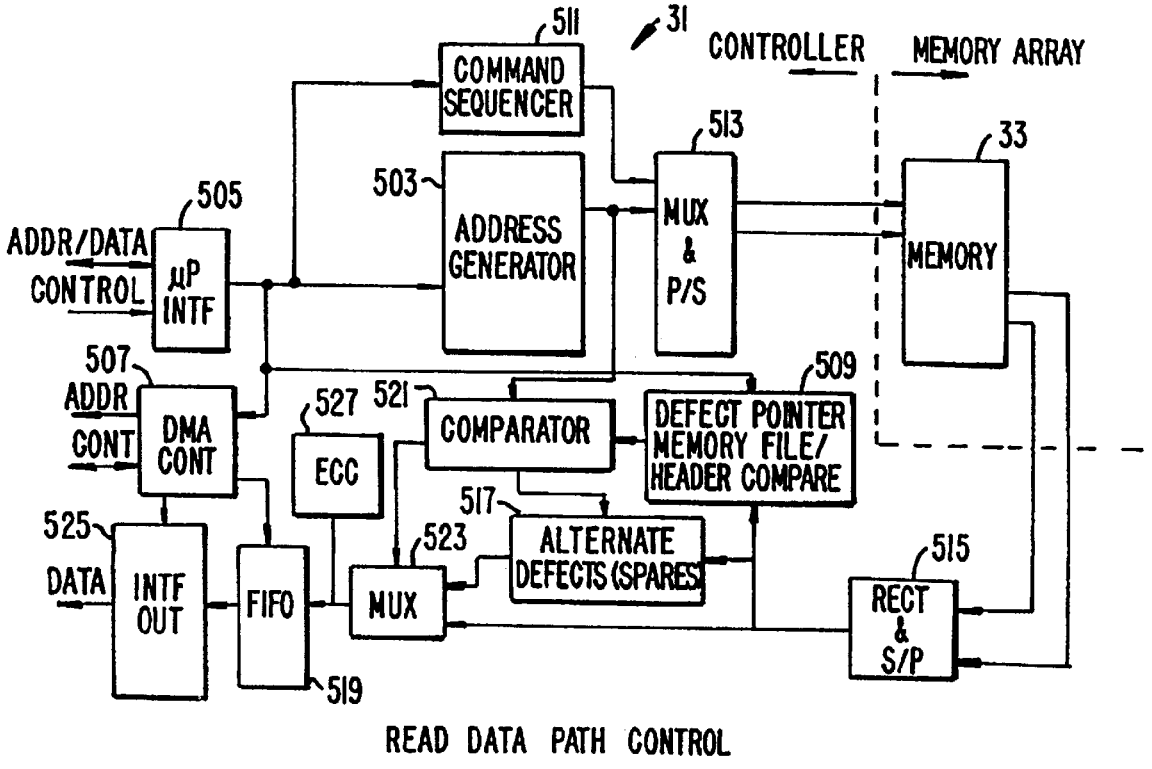

511
31
CONTROLLER
MEMORY ARRAY
COMMAND SEQUENCER
513
33
503
ADDRESS GENERATOR
MUX & P/S
MEMORY
505
ADDR/DATA
CONTROL
μP INTF
507
ADDR
CONT
DMA CONT
527
521
509
ECC
COMPARATOR
DEFECT POINTER MEMORY FILE/ HEADER COMPARE
517
525
523
515
DATA
INTF OUT
FIFO
MUX
ALTERNATE DEFECTS (SPARES)
RECT & S/P
519
READ DATA PATH CONTROL

FIG._6

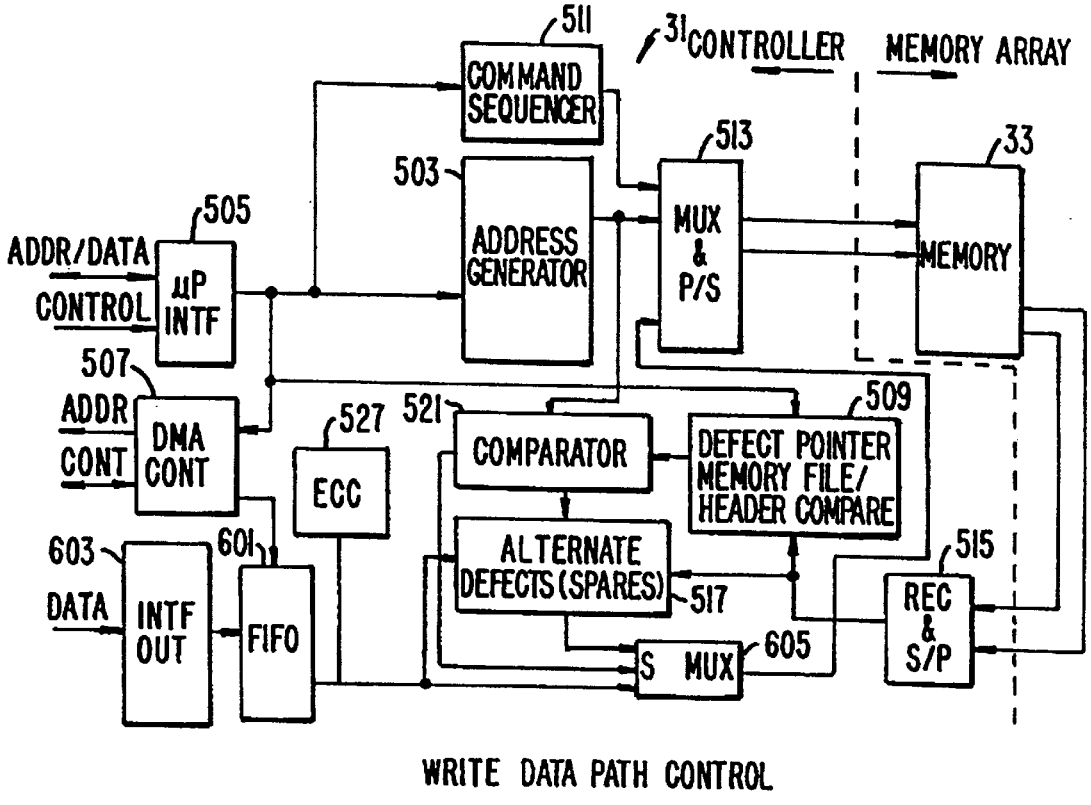

511
31
CONTROLLER
MEMORY ARRAY
COMMAND SEQUENCER
513
33
503
ADDRESS GENERATOR
MUX & P/S
MEMORY
505
ADDR/DATA
CONTROL
µP INTF
507
ADDR
CONT
DMA CONT
527
521
509
ECC
COMPARATOR
DEFECT POINTER MEMORY FILE/ HEADER COMPARE
603
601
515
DATA
INTF OUT
FIFO
ALTERNATE DEFECTS (SPARES)
517
REC & S/P
S MUX
605
WRITE DATA PATH CONTROL

FIG._7

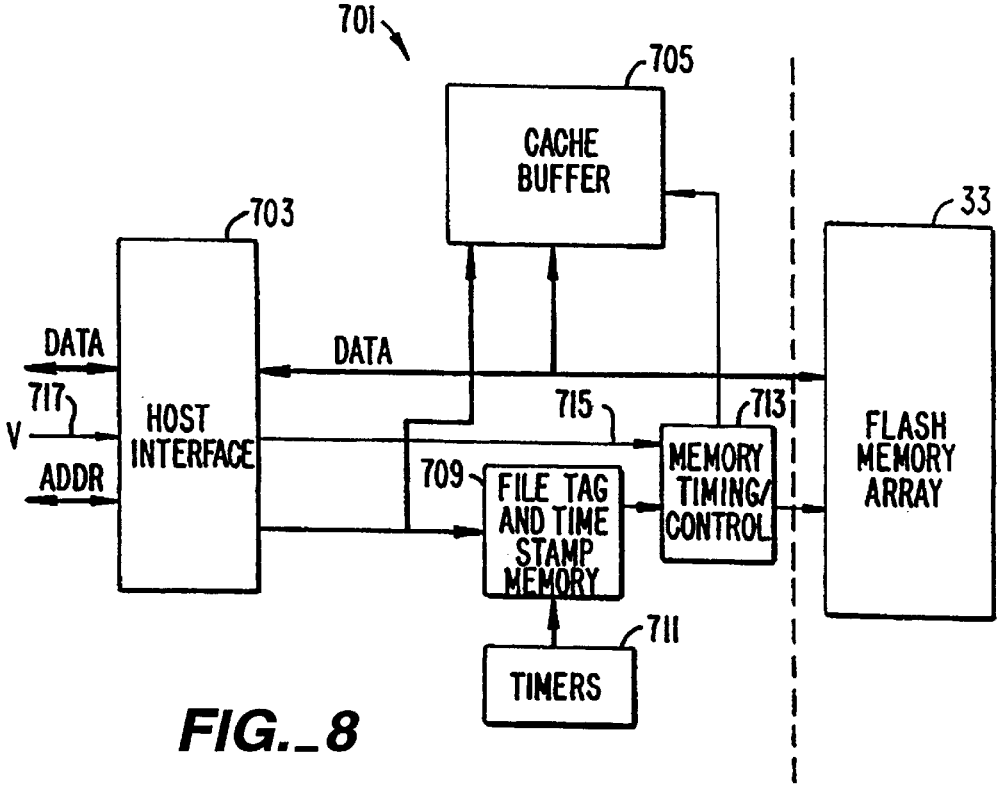

701
705
CACHE BUFFER
703
33
DATA
DATA
717
V
ADDR
HOST INTERFACE
715
713
709
FILE TAG AND TIME STAMP MEMORY
MEMORY TIMING/ CONTROL
FLASH MEMORY ARRAY
711
TIMERS

FIG._8

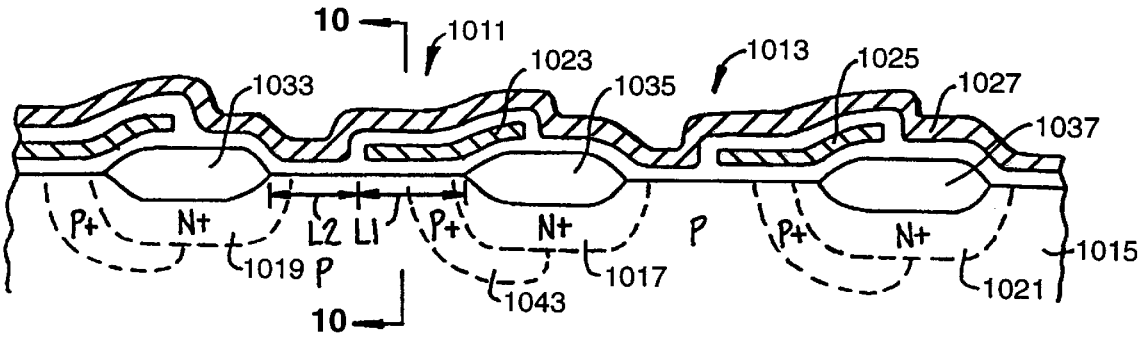


FIG._9

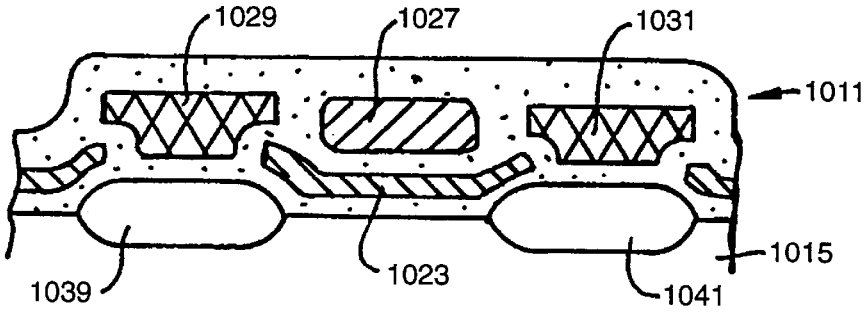


FIG._10

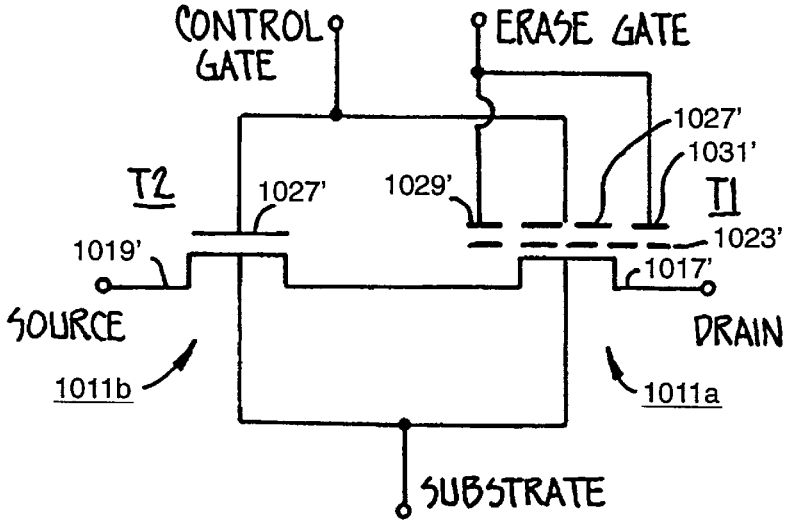


FIG._11

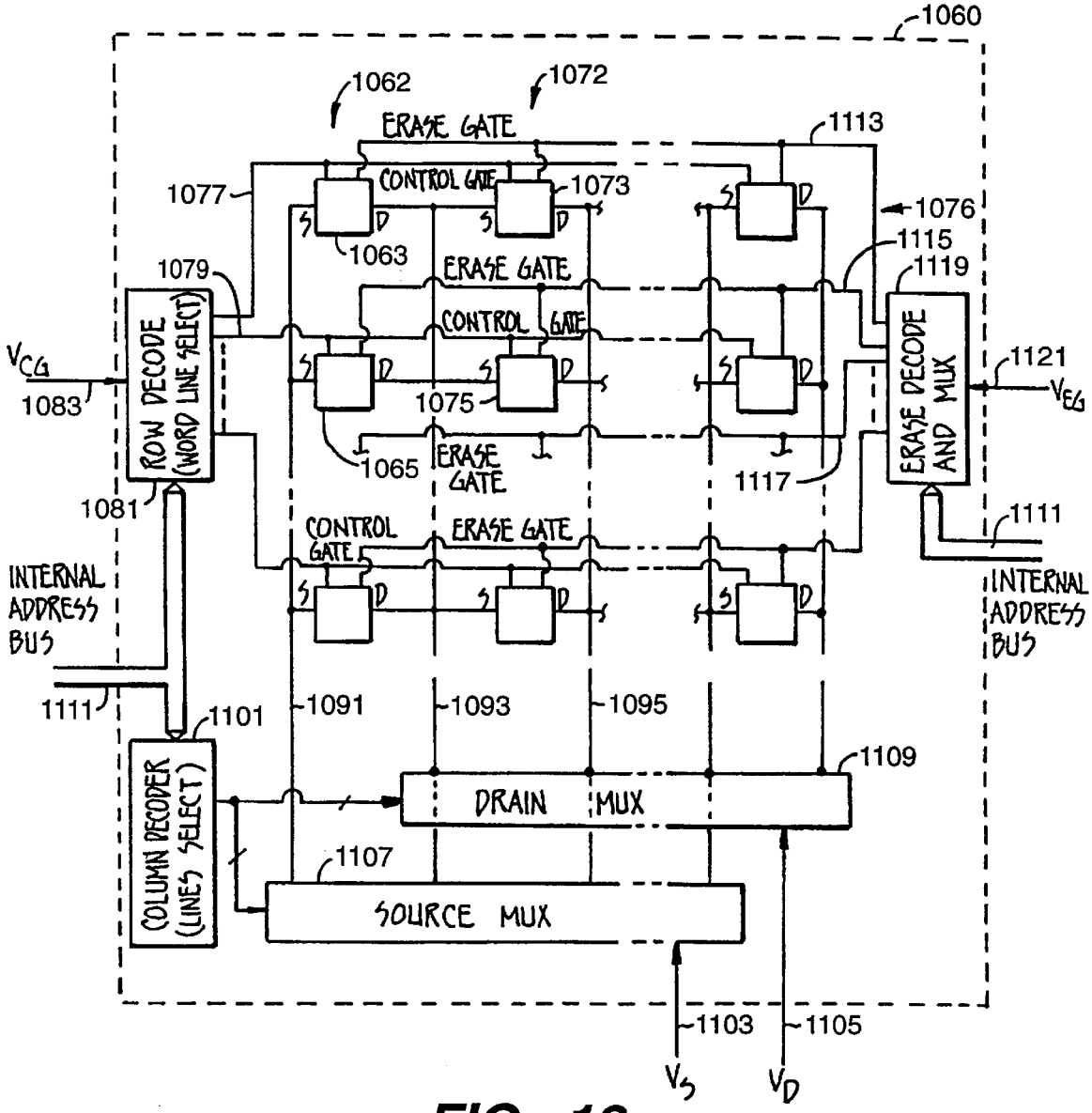

1060
1062
1072
ERASE GATE
1113
CONTROL GATE
1073
1077
1076
1063
1115
1119
1079
ERASE GATE
CONTROL GATE
ROW DECODE (WORD LINE SELECT)
ERASE DECODE AND MUX
V_{CG}
1083
1075
1121
V_{EG}
1065
ERASE GATE
1117
1081
CONTROL GATE
ERASE GATE
1111
INTERNAL ADDRESS BUS
INTERNAL ADDRESS BUS
1111
1101
1091
1093
1095
1109
COLUMN DECODER (LINES SELECT)
DRAIN MUX
1107
SOURCE MUX
1103
1105
V_S
V_D

FIG._12

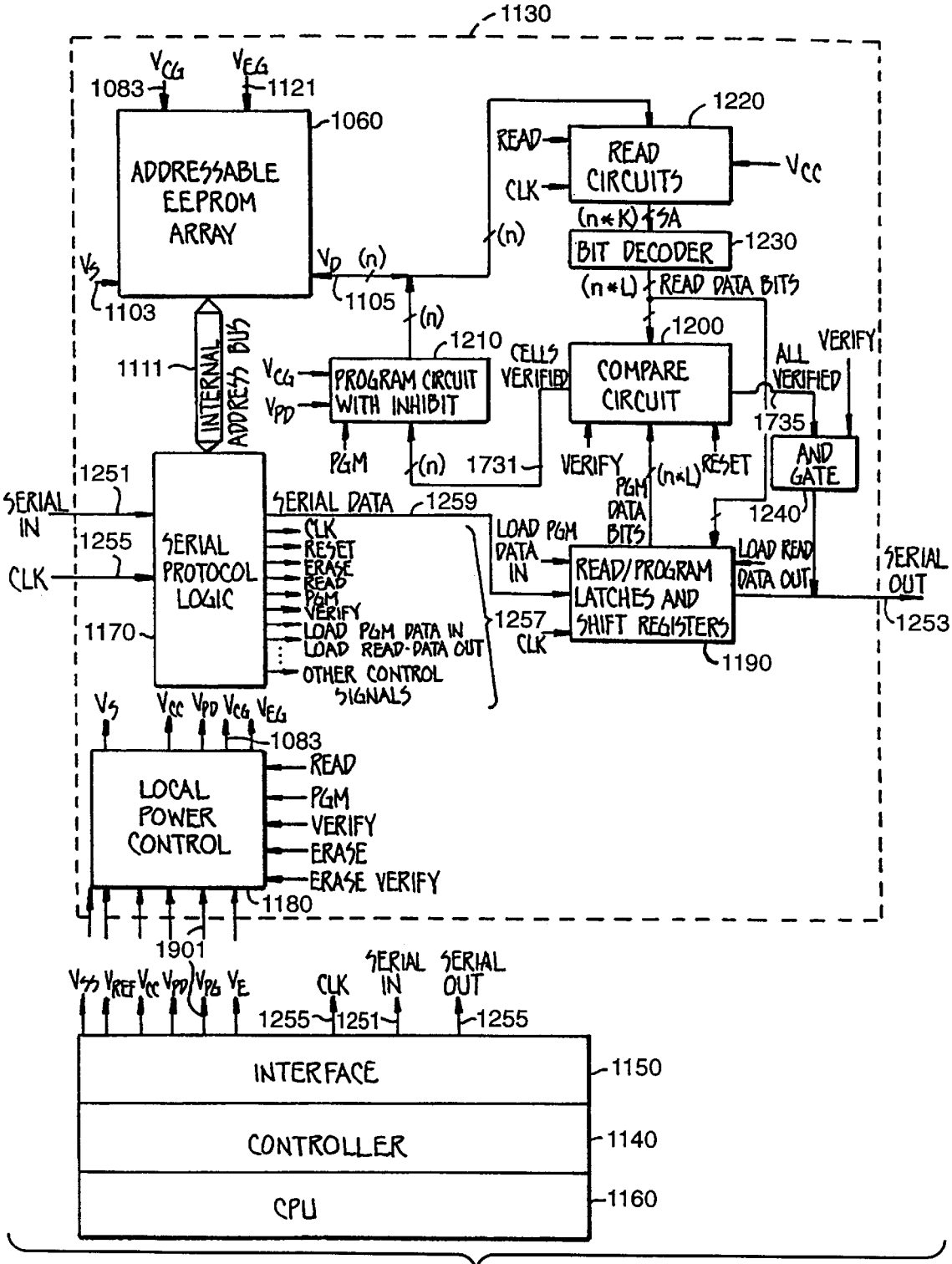

1130
V_{CG}
V_{EG}
1083
1121
ADDRESSABLE EEPROM ARRAY
1060
READ
CLK
READ CIRCUITS
1220
V_{CC}
(n*K) SA
BIT DECODER
1230
(n*L) READ DATA BITS
V_S
1103
V_D (n)
1105
(n)
1200
VERIFY
1111
INTERNAL ADDRESS BUS
V_{CG}
V_{PD}
PROGRAM CIRCUIT WITH INHIBIT
1210
CELLS VERIFIED
COMPARE CIRCUIT
ALL VERIFIED
1735
AND GATE
PGM
(n) 1731
VERIFY
(n*L)
RESET
1240
1251
SERIAL IN
1255
CLK
SERIAL PROTOCOL LOGIC
1170
SERIAL DATA
1259
CLK
RESET
ERASE
READ
PGM
VERIFY
LOAD PGM DATA IN
LOAD READ-DATA OUT
OTHER CONTROL SIGNALS
LOAD PGM DATA IN
PGM DATA BITS
READ/PROGRAM LATCHES AND SHIFT REGISTERS
LOAD READ DATA OUT
SERIAL OUT
1253
1257
CLK
1190
V_S
V_{CC} V_{PD} V_{CG} V_{EG}
1083
LOCAL POWER CONTROL
READ
PGM
VERIFY
ERASE
ERASE VERIFY
1180
1901
V_{SS} V_{REF} V_{CC} V_{PD} V_{PG} V_E
CLK
SERIAL IN
SERIAL OUT
1255
1251
1255
INTERFACE
1150
CONTROLLER
1140
CPU
1160

FIG._13

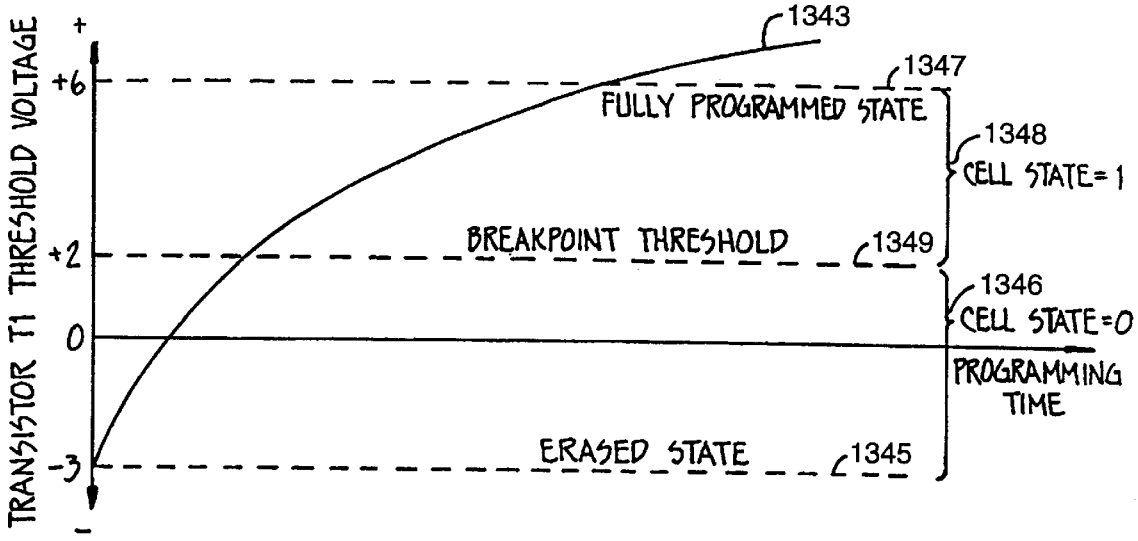


FIG._14

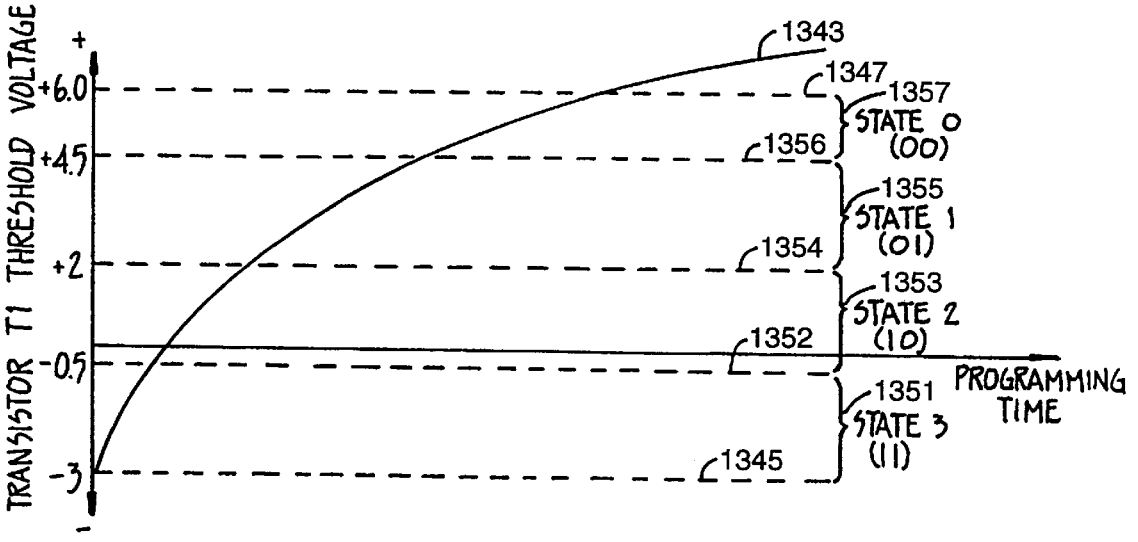


FIG._15A

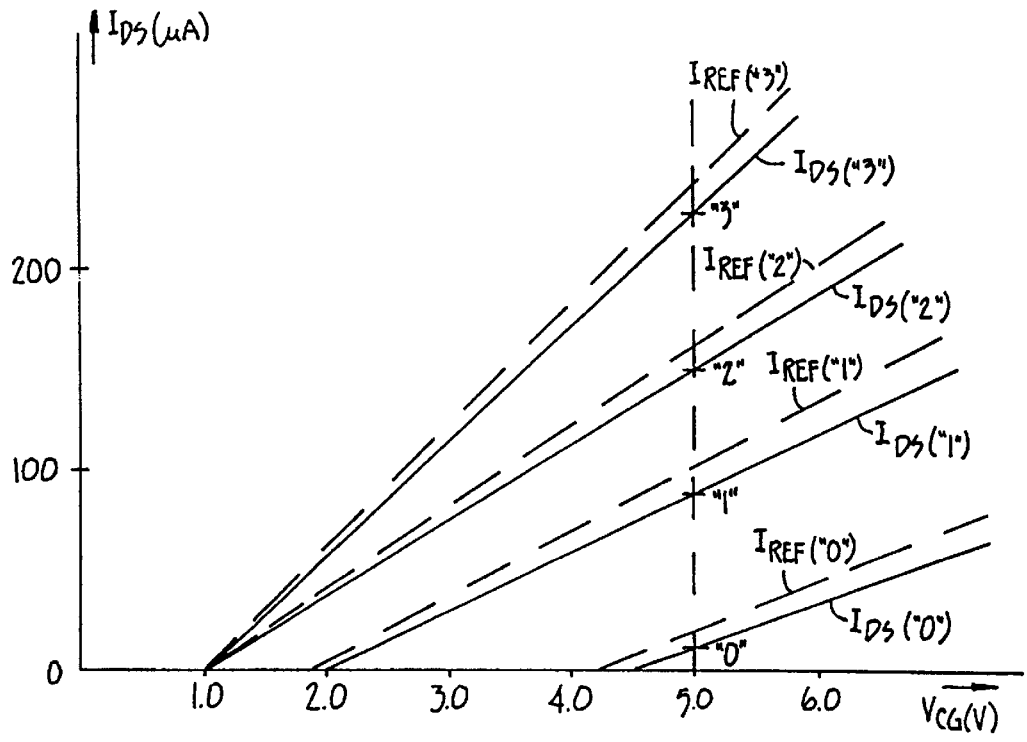


FIG._15B

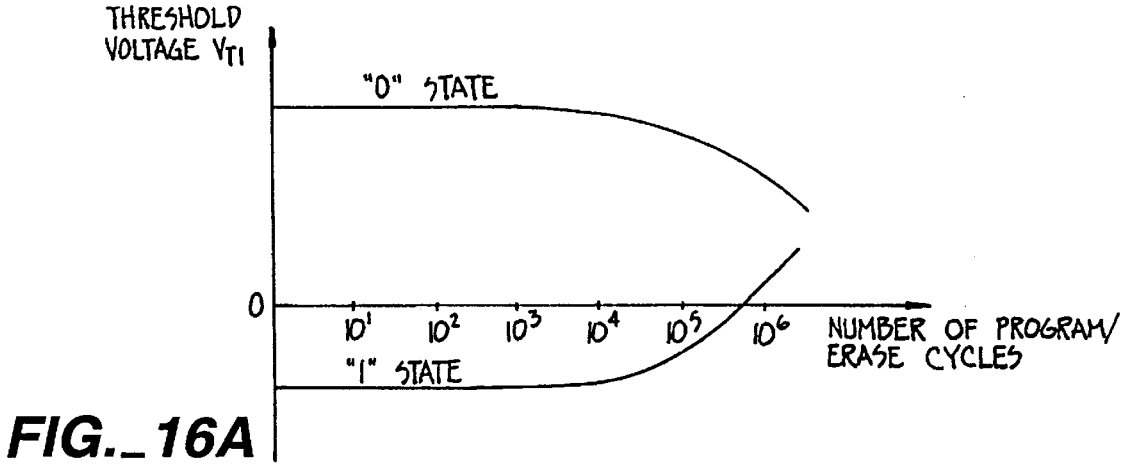


FIG._16A

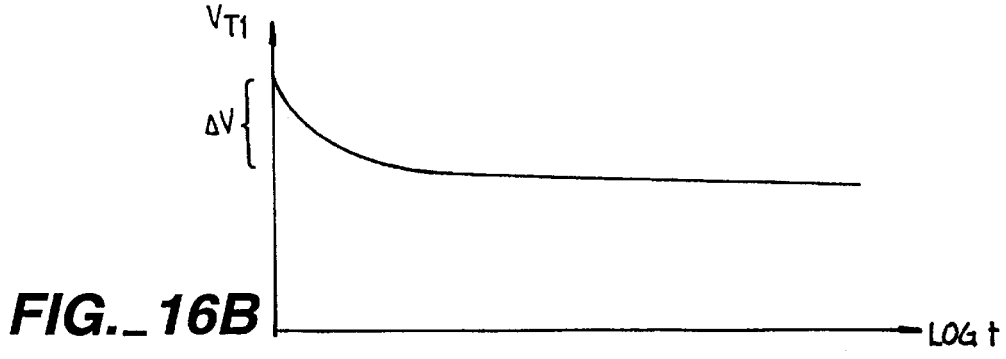


FIG._16B

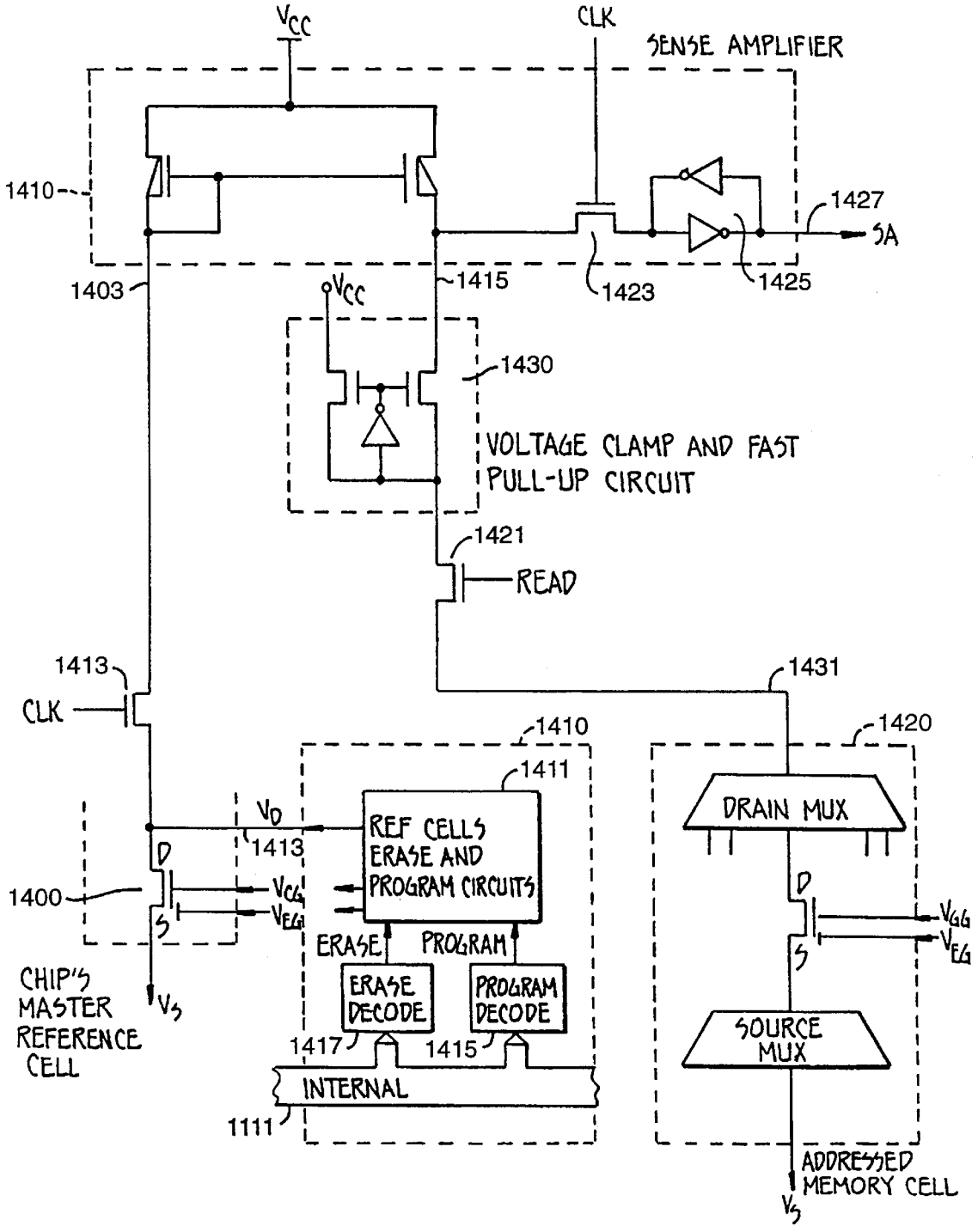

V_{CC}
CLK
SENSE AMPLIFIER
1410
1427
SA
1403
1415
1423
1425
V_{CC}
1430
VOLTAGE CLAMP AND FAST PULL-UP CIRCUIT
1421
READ
1413
CLK
1431
1410
1420
1411
V_D
1413
REF CELLS ERASE AND PROGRAM CIRCUITS
DRAIN MUX
D
1400
V_{GG}
V_{EG}
S
ERASE
PROGRAM
ERASE DECODE
PROGRAM DECODE
CHIP'S MASTER REFERENCE CELL
V_S
1417
1415
INTERNAL
SOURCE MUX
1111
ADDRESSED MEMORY CELL
V_S

FIG._17A

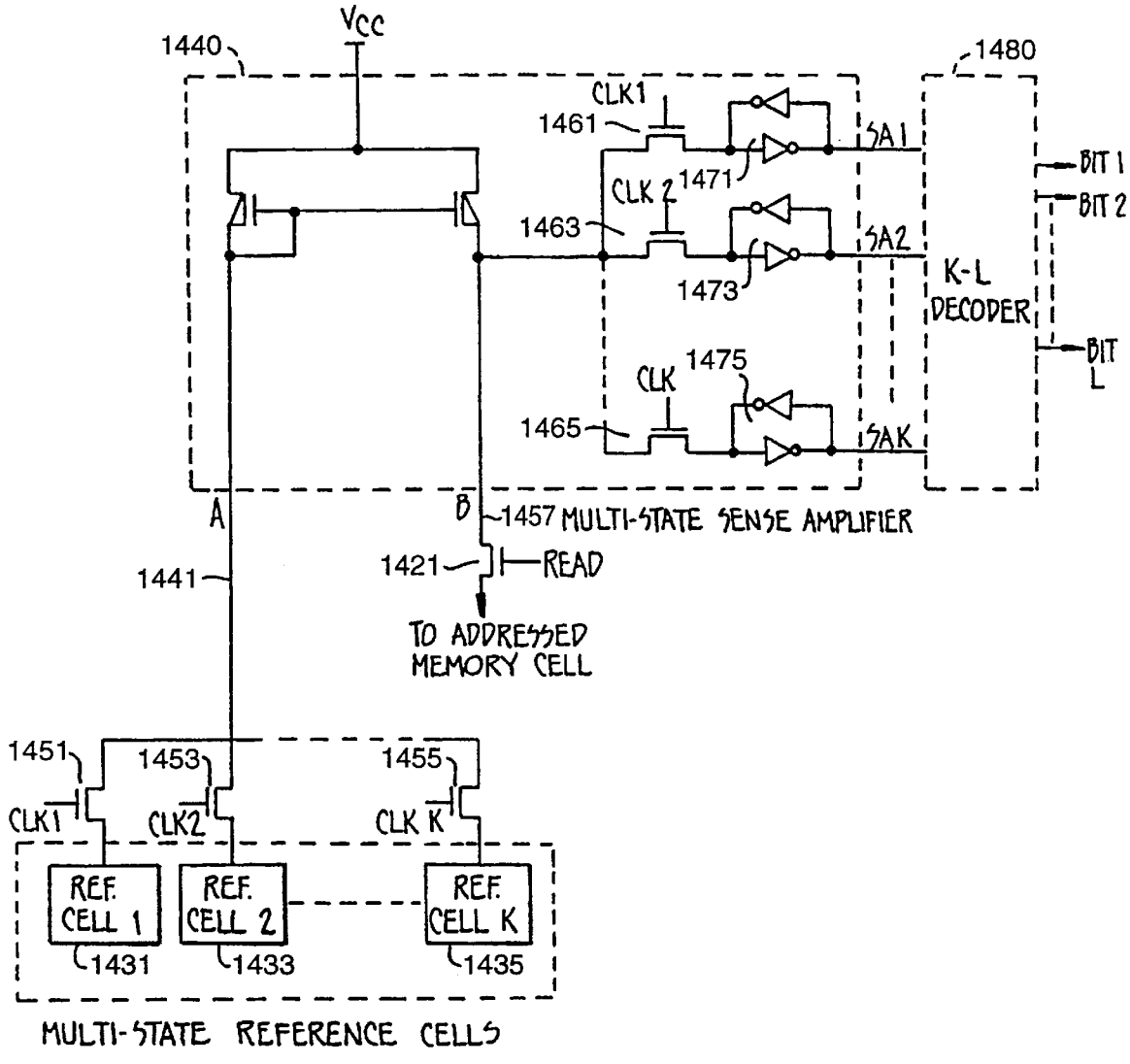

Vcc
1440
1480
CLK1
1461
SA1
BIT 1
BIT 2
CLK 2
1471
1463
SA2
1473
K-L
DECODER
CLK
1475
BIT
L
1465
SAK
A
B
1457 MULTI-STATE SENSE AMPLIFIER
1421
READ
1441
TO ADDRESSED
MEMORY CELL
1451
1453
1455
CLK1
CLK2
CLK K
REF.
CELL 1
REF.
CELL 2
REF.
CELL K
1431
1433
1435
MULTI-STATE REFERENCE CELLS

FIG._17B

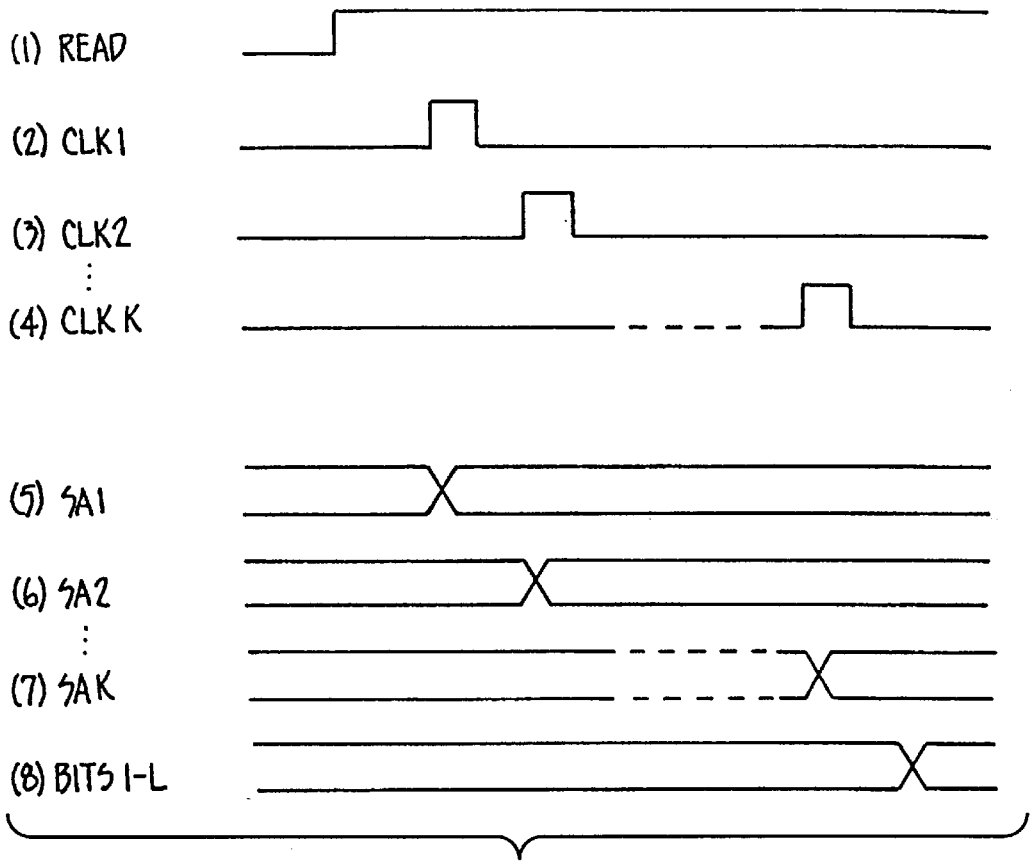


FIG._17C

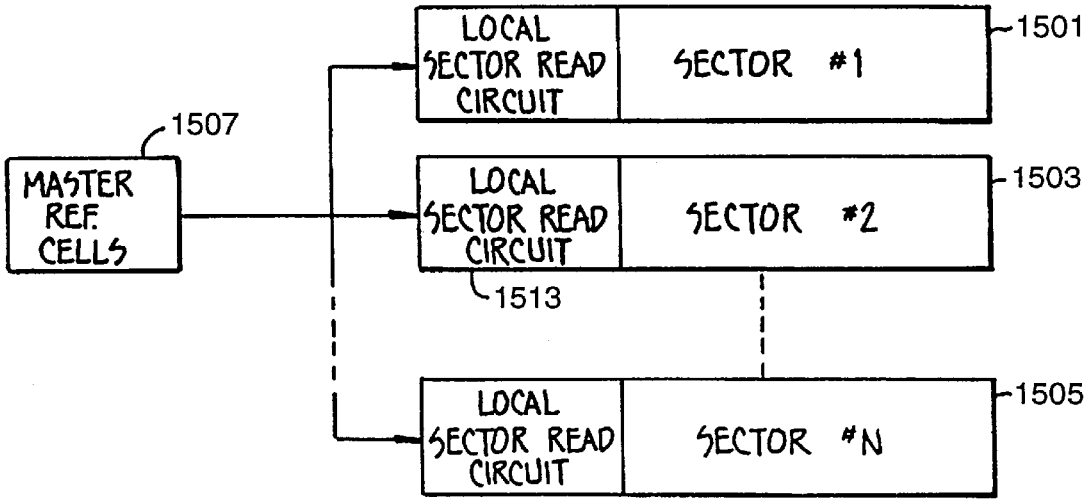


FIG._18

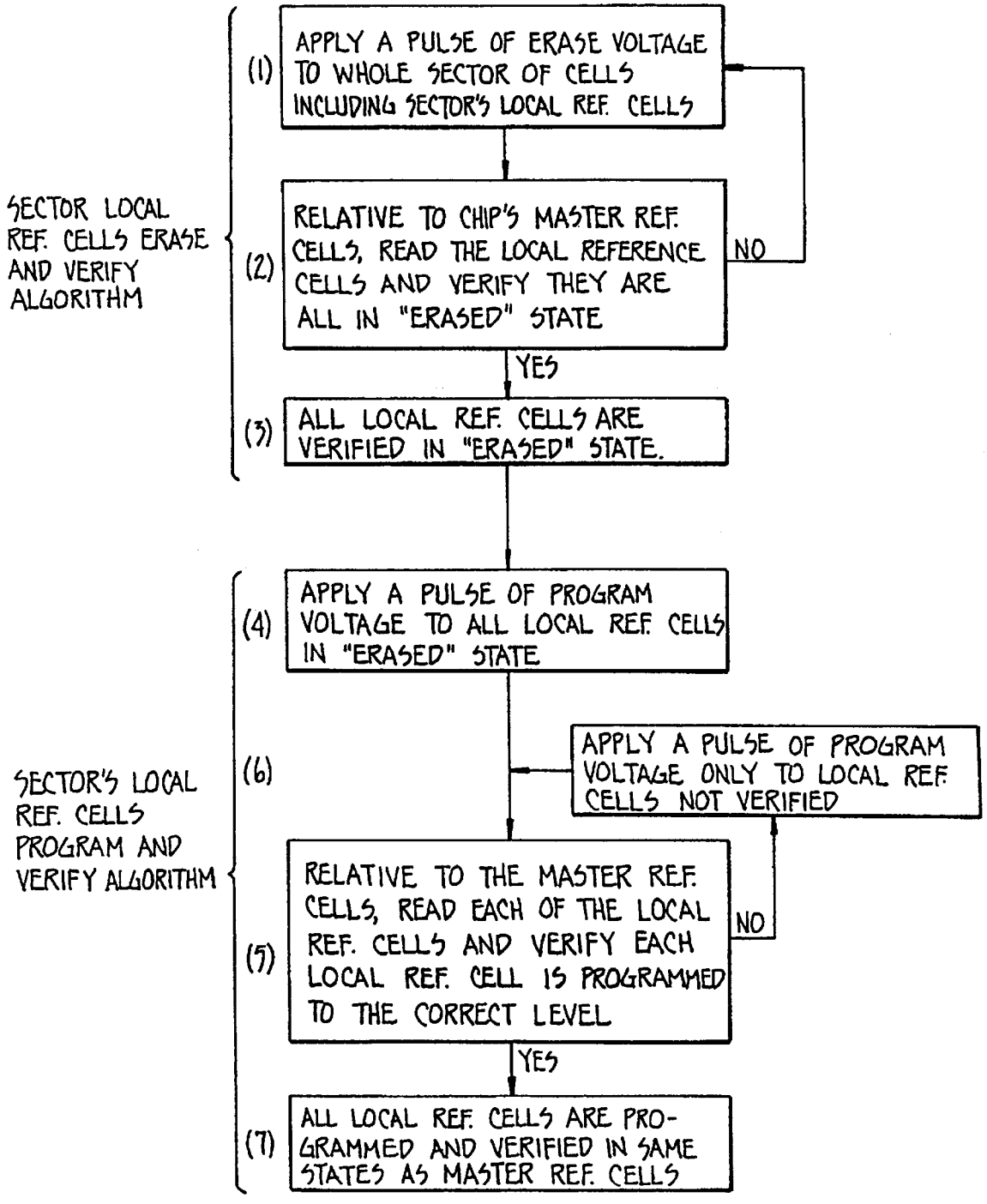

SECTOR LOCAL REF. CELLS ERASE AND VERIFY ALGORITHM
(1) APPLY A PULSE OF ERASE VOLTAGE TO WHOLE SECTOR OF CELLS INCLUDING SECTOR'S LOCAL REF. CELLS
(2) RELATIVE TO CHIP'S MASTER REF. CELLS, READ THE LOCAL REFERENCE CELLS AND VERIFY THEY ARE ALL IN "ERASED" STATE
NO
YES
(3) ALL LOCAL REF. CELLS ARE VERIFIED IN "ERASED" STATE.
SECTOR'S LOCAL REF. CELLS PROGRAM AND VERIFY ALGORITHM
(4) APPLY A PULSE OF PROGRAM VOLTAGE TO ALL LOCAL REF. CELLS IN "ERASED" STATE
(6) APPLY A PULSE OF PROGRAM VOLTAGE ONLY TO LOCAL REF. CELLS NOT VERIFIED
(5) RELATIVE TO THE MASTER REF. CELLS, READ EACH OF THE LOCAL REF. CELLS AND VERIFY EACH LOCAL REF. CELL IS PROGRAMMED TO THE CORRECT LEVEL
NO
YES
(7) ALL LOCAL REF. CELLS ARE PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CELLS

FIG._19

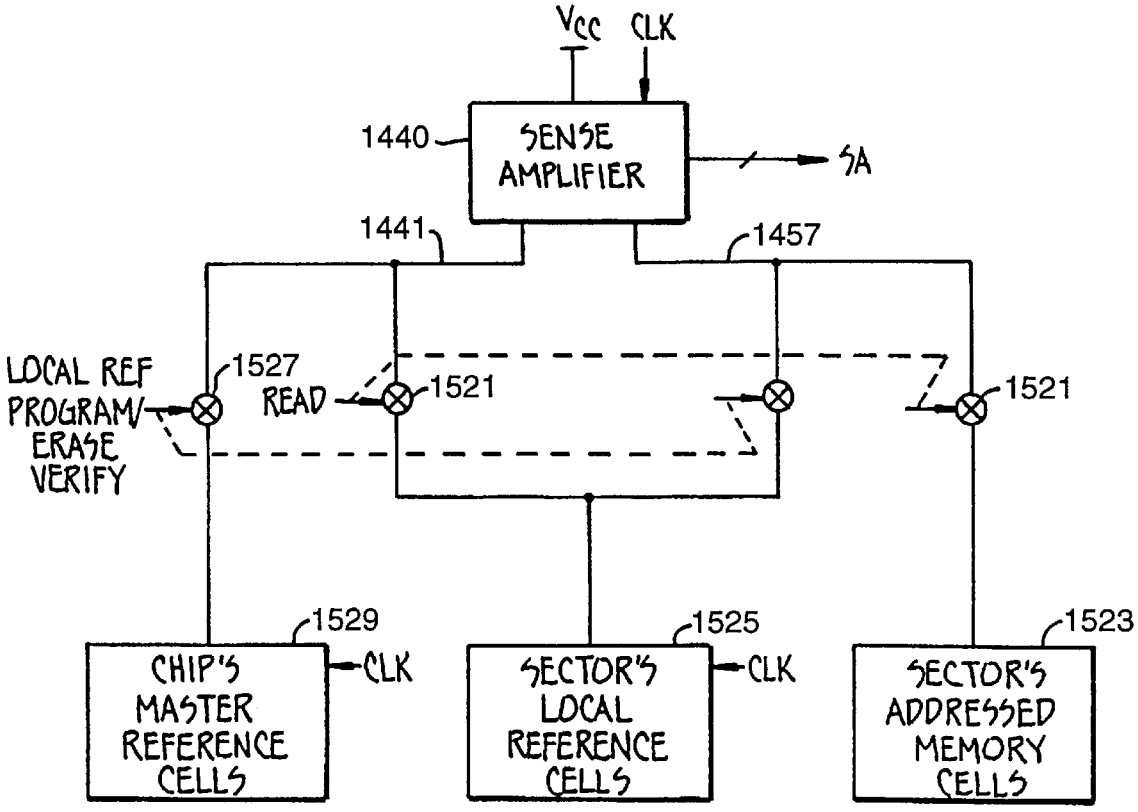


FIG._20A

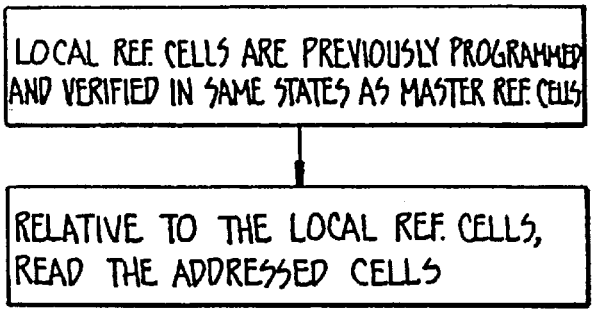
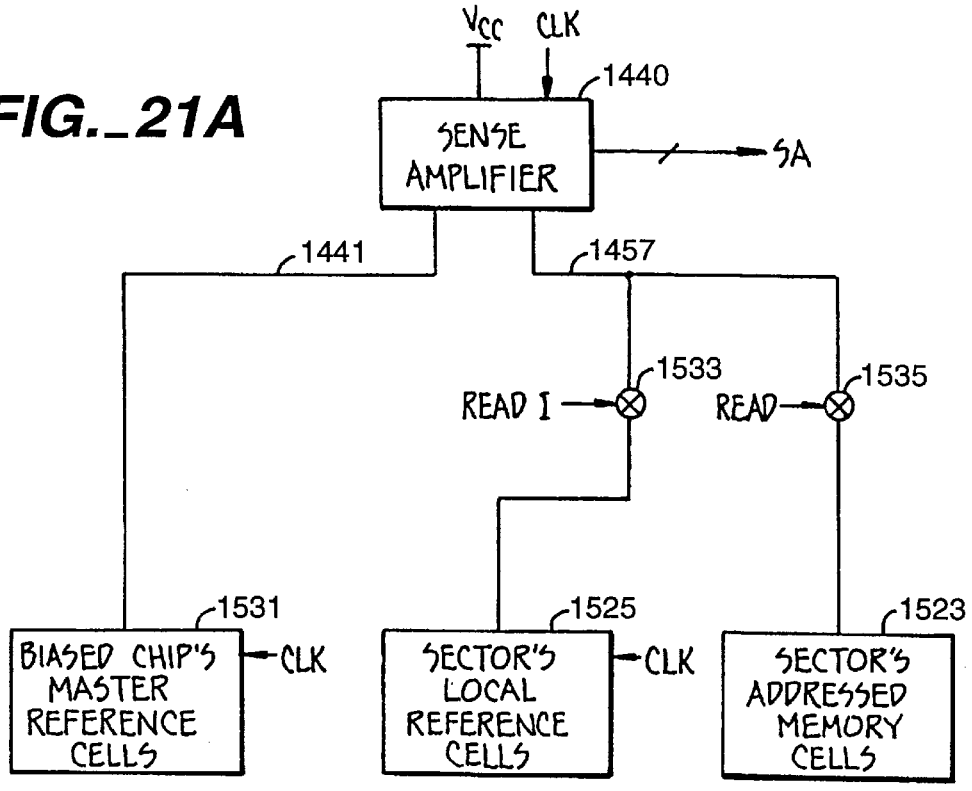


FIG._20B

FIG._21A



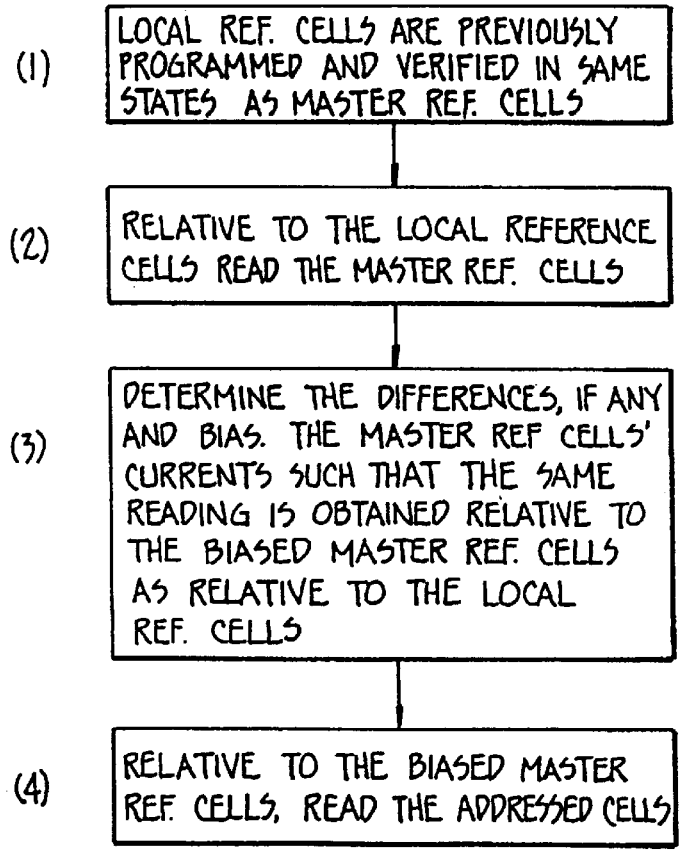


FIG._21D

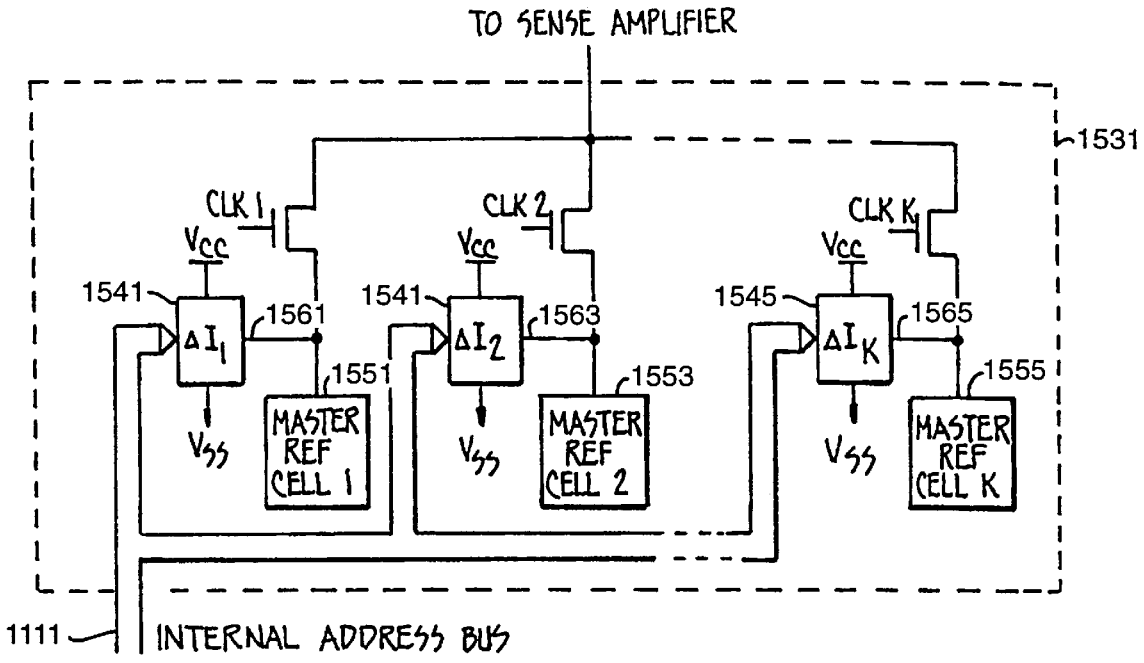


FIG._21B

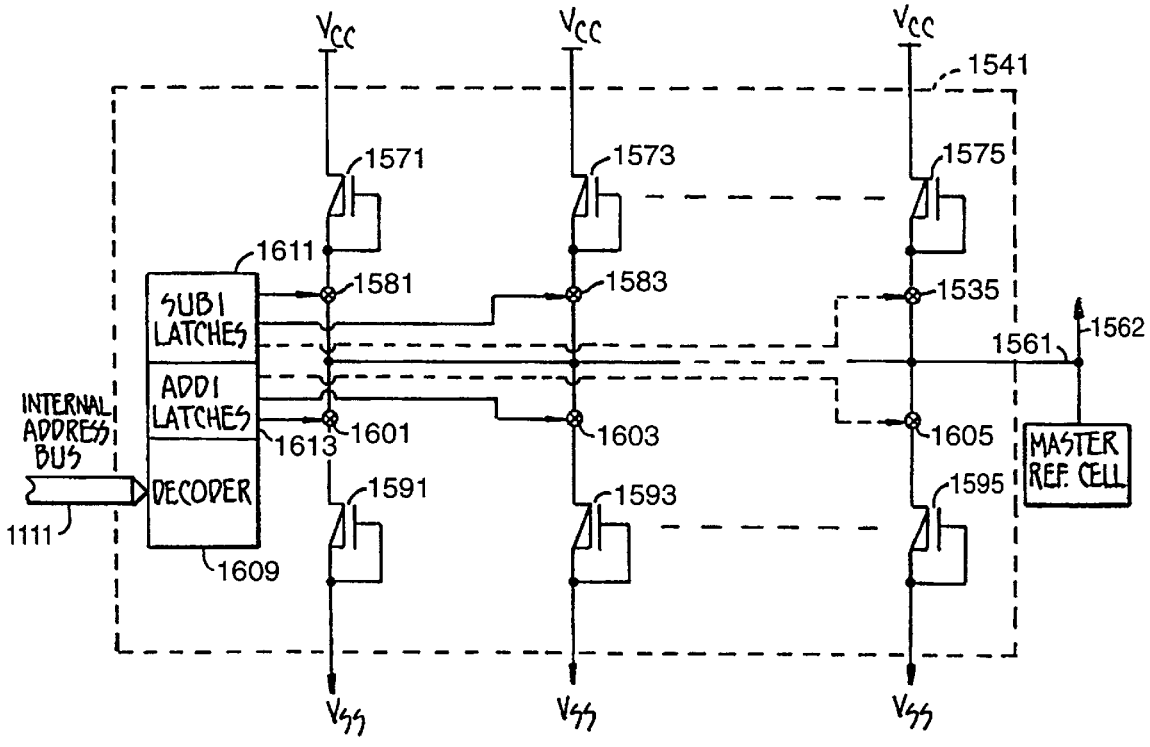
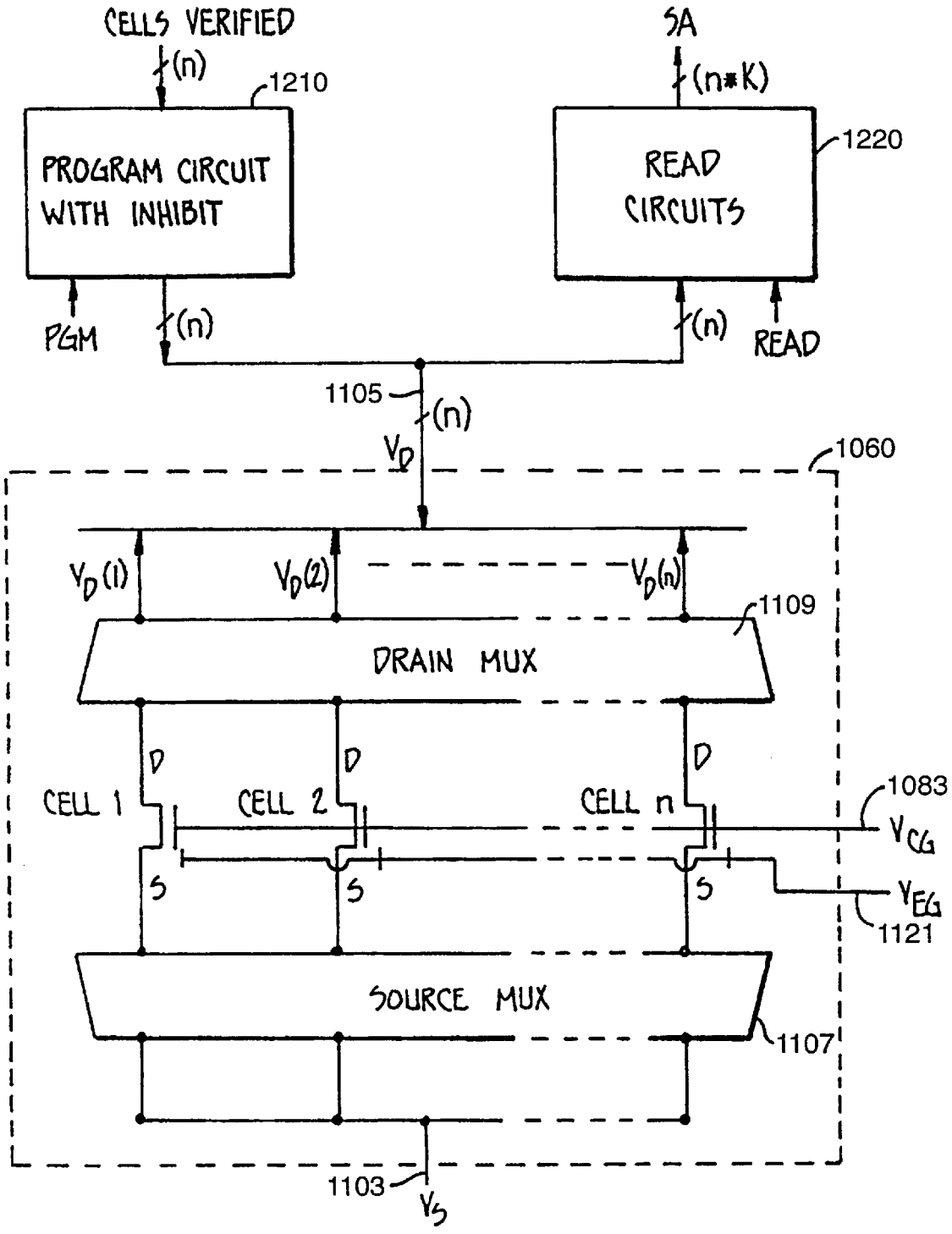
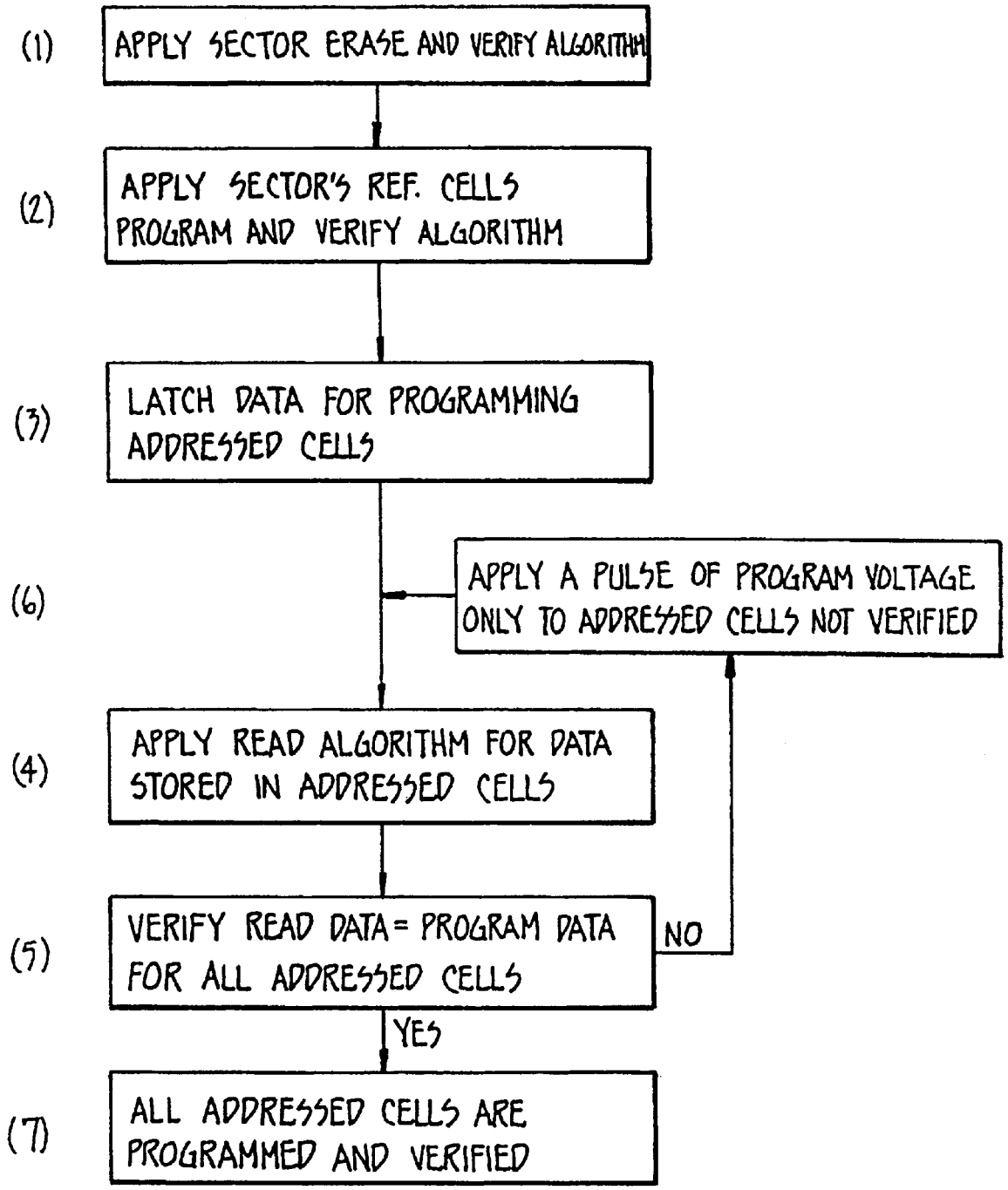


FIG._21C



READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG._22



PROGRAM ALGORITHM

FIG._23

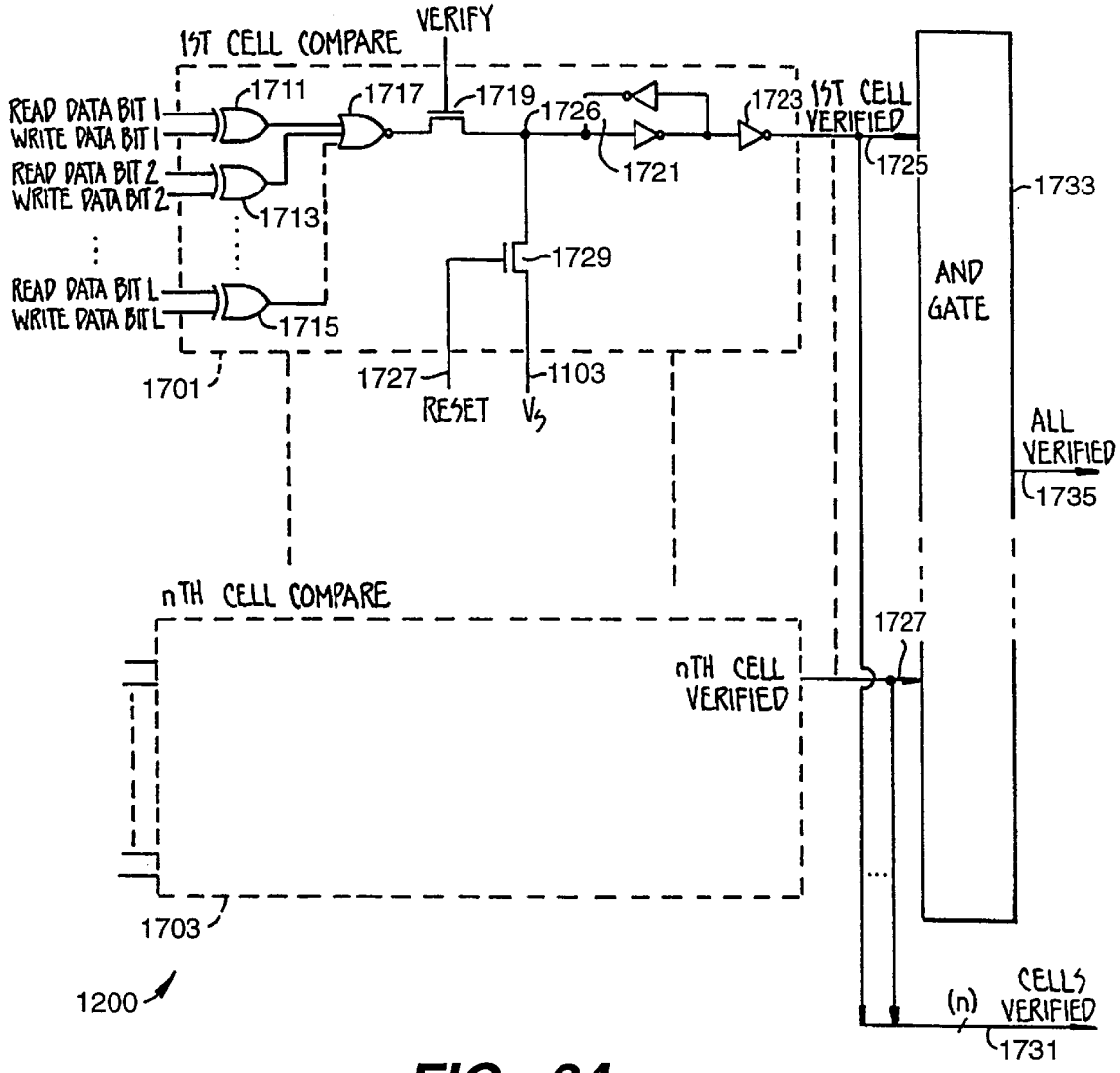

VERIFY
1ST CELL COMPARE
READ DATA BIT 1
WRITE DATA BIT 1
READ DATA BIT 2
WRITE DATA BIT 2
READ DATA BIT L
WRITE DATA BIT L
1711
1717
1719
1726
1723
1721
1725
1733
1713
1729
1715
1701
1727
1103
RESET
Vs
1ST CELL VERIFIED
AND GATE
ALL VERIFIED
1735
nTH CELL COMPARE
1727
nTH CELL VERIFIED
1703
1200
(n) CELLS VERIFIED
1731

FIG._24

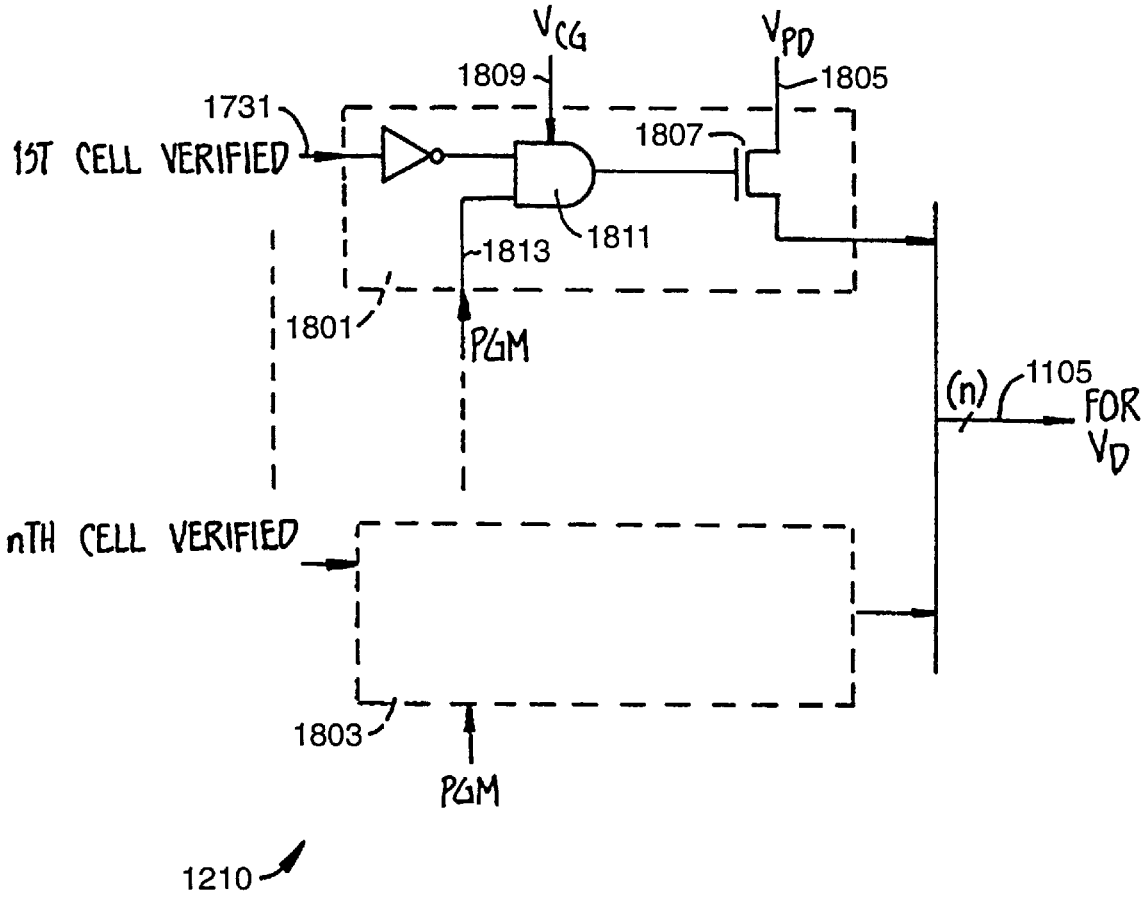

V_{CG}
V_{PD}
1809
1805
1731
1807
1ST CELL VERIFIED
1811
1813
1801
PGM
(n)
1105
FOR V_D
nTH CELL VERIFIED
1803
PGM
1210

FIG._25

	SELECTED CONTROL GATE V_{CG}	DRAIN V_D	SOURCE V_S	ERASE GATE V_{EG}
READ	V_{PG}	V_{REF}	V_{SS}	V_E
PROGRAM	V_{PG}	V_{PD}	V_{SS}	V_E
PROGRAM VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E

TABLE 1

FIG._26

(TYPICAL VALUES)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V_{PG}	V_{CC}	12V	$V_{CC}+\delta V$	V_{CC}	$V_{CC}-\delta V$
V_{CC}	5V	5V	5V	5V	5V
V_{PD}	V_{SS}	8V	8V	V_{SS}	V_{SS}
V_E	V_{SS}	V_{SS}	V_{SS}	20V	V_{SS}
UNSELECTED CONTROL GATE	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
UNSELECTED BIT LINE	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}

V_{SS}=0V, V_{REF}=1.5V, δV=0.5V - 1V

TABLE 2

FIG._27

FLASH EEPROM SYSTEM WITH CELL BY CELL PROGRAMMING VERIFICATION

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a continuation of patent application Ser. No. 08/174,768, filed Dec. 29, 1993, now U.S. Pat. No. 5,602,987 which in turn is a continuation of patent application Ser. No. 07/963,838, filed Oct. 20, 1992, now U.S. Pat. No. 5,297,148, which in turn is a division of patent application Ser. No. 07/337,566, filed Apr. 13, 1989, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates generally to semiconductor electrically erasable programmable read only memories (EEprom), and specifically to a system of integrated circuit Flash EEprom chips.

Computer systems typically use magnetic disk drives for mass storage of data. However, disk drives are disadvantageous in that they are bulky and in their requirement for high precision moving mechanical parts. Consequently they are not rugged and are prone to reliability problems, as well as consuming significant amounts of power. Solid state memory devices such as DRAM's and SRAM's do not suffer from these disadvantages. However, they are much more expensive, and require constant power to maintain their memory (volatile). Consequently, they are typically used as temporary storage.

EEprom's and Flash EEprom's are also solid state memory devices. Moreover, they are nonvolatile, and retain their memory even after power is shut down. However, conventional Flash EEprom's have a limited lifetime in terms of the number of write (or program)/erase cycles they can endure. Typically the devices are rendered unreliable after 10^2 to 10^3 write/erase cycles. Traditionally, they are typically used in applications where semi-permanent storage of data or program is required but with a limited need for reprogramming.

Accordingly, it is an object of the present invention to provide a Flash EEprom memory system with enhanced performance and which remains reliable after enduring a large number of write/erase cycles.

It is another object of the present invention to provide an improved Flash EEprom system which can serve as non-volatile memory in a computer system.

It is another object of the present invention to provide an improved Flash EEprom system that can replace magnetic disk storage devices in computer systems.

It is another object of the present invention to provide a Flash EEprom system with improved erase operation.

It is another object of the present invention to provide a Flash EEprom system with improved error correction.

It is yet another object of the present invention to provide a Flash EEprom with improved write operation that minimizes stress to the Flash EEprom device.

It is still another object of the present invention to provide a Flash EEprom system with enhanced write operation.

SUMMARY OF THE INVENTION

These and additional objects are accomplished by improvements in the architecture of a system of EEprom chips, and the circuits and techniques therein.

According to one aspect of the present invention, an array of Flash EEprom cells on a chip is organized into sectors

such that all cells within each sector are erasable at once. A Flash EEprom memory system comprises one or more Flash EEprom chips under the control of a controller. The invention allows any combination of sectors among the chips to be selected and then erased simultaneously. This is faster and more efficient than prior art schemes where all the sectors must be erased every time or only one sector at a time can be erased. The invention further allows any combination of sectors selected for erase to be deselected and prevented from further erasing during the erase operation. This feature is important for stopping those sectors that are first to be erased correctly to the "erased" state from over erasing, thereby preventing unnecessary stress to the Flash EEprom device. The invention also allows a global de-select of all sectors in the system so that no sectors are selected for erase. This global reset can quickly put the system back to its initial state ready for selecting the next combination of sectors for erase. Another feature of the invention is that the selection is independent of the chip select signal which enables a particular chip for read or write operation. Therefore it is possible to perform an erase operation on some of the Flash EEprom chips while read and write operations may be performed on other chips not involved in the erase operation.

According to another aspect of the invention, improved error correction circuits and techniques are used to correct for errors arising from defective Flash EEprom memory cells. One feature of the invention allows defect mapping at cell level in which a defective cell is replaced by a substitute cell from the same sector. The defect pointer which connects the address of the defective cell to that of the substitute cell is stored in a defect map. Every time the defective cell is accessed, its bad data is replaced by the good data from the substitute cell.

Another feature of the invention allows defect mapping at the sector level. When the number of defective cells in a sector exceeds a predetermined number, the sector containing the defective cells is replaced by a substitute sector.

An important feature of the invention allows defective cells or defective sectors to be remapped as soon as they are detected thereby enabling error correction codes to adequately rectify the relatively few errors that may crop up in the system.

According to yet another aspect of the present invention, a write cache is used to minimize the number of writes to the Flash EEprom memory. In this way the Flash EEprom memory will be subject to fewer stress inducing write/erase cycles, thereby retarding its aging. The most active data files are written to the cache memory instead of the Flash EEprom memory. Only when the activity levels have reduced to a predetermined level are the data files written from the cache memory to the Flash EEprom memory. Another advantage of the invention is the increase in write throughput by virtue of the faster cache memory.

According to yet another aspect of the present invention, one or more printed circuit cards are provided which contain controller and EEprom circuit chips for use in a computer system memory for long term, non-volatile storage, in place of a hard disk system, and which incorporate various of the other aspects of this invention alone and in combination.

The present invention also includes improvements in EEprom array read and write circuits and techniques in order to provide multiple threshold levels that allow accurate reading and writing of more than two distinct states within each memory cell over an extended lifetime of the memory cells, so that more than one bit may be reliably stored in each cell.

According to one aspect of the present invention, the multiple threshold breakpoint levels are provided by a set of memory cells which serves as master reference cells. The master reference cells are independently and externally programmable, either by the memory manufacturer or the user. This feature provides maximum flexibility, allowing the breakpoint thresholds to be individually set within the threshold window of the device at any time. Also, by virtue of being an identical device as that of the memory cells, the reference cells closely track the same variations due to manufacturing processes, operating conditions and device aging. The independent programmability of each breakpoint threshold level allows optimization and fine-tuning of the threshold window's partitioning, critical in multi-state implementation. Furthermore, it allows post-manufacture configuration for either 2-state or multi-state memory from the same device, depending on user need or device characteristics at the time.

According to another aspect of the present invention, a set of memory cells within each sector (where a sector is a group of memory cells which are all erased at the same time in a Flash EEprom) are set aside as local reference cells. Each set of reference cells tracks the Flash cells in the same sector closely as they are both cycled through the same number of program/erase cycles. Thus, the aging that occurs in the memory cells of a sector after a large number of erase/reprogram cycles is also reflected in the local reference cells. Each time the sector of flash cells is erased and reprogrammed, the set of individual breakpoint threshold levels are re-programmed to the associated local reference cells. The threshold levels read from the local reference cells then automatically adjust to changing conditions of the memory cells of the same sector. The threshold window's partitioning is thus optimally maintained. This technique is also useful for a memory that employs only a single reference cell that is used to read two state (1 bit) memory cells.

According to another aspect of the present invention, the threshold levels rewritten at each cycle to the local reference cells are obtained from a set of master cells which are not cycled along with the memory cells but rather which retain a charge that has been externally programmed (or reprogrammed). Only a single set of master memory cells is needed for an entire memory integrated circuit.

In one embodiment, the read operation directly uses the threshold levels in the local reference cells previously copied from the master reference cells. In another embodiment, the read operation indirectly uses the threshold levels in the local reference cells even though the reading is done relative to the master reference cells. It does this by first reading the local reference cells relative to the master reference cells. The differences detected are used to offset subsequent regular readings of memory cells relative to the master reference cells so that the biased readings are effectively relative to the local reference cells.

According to another aspect of the present invention, the program and verify operations are performed on a chunk (i.e. several bytes) of addressed cells at a time. Furthermore, the verify operation is performed by circuits on the EEprom chip. This avoids delays in shipping data off chip serially for verification in between each programming step.

According to another aspect of the present invention, where a programmed state is obtained by repetitive steps of programming and verifying from the "erased" state, a circuit verifies the programmed state after each programming step with the intended state and selectively inhibits further programming of any cells in the chunk that have been verified to have been programmed correctly. This enables efficient parallel programming of a chunk of data in a multi-state implementation.

According to another aspect of the present invention, where a chunk of EEprom cells are addressed to be erased in parallel, an erased state is obtained by repetitive steps of erasing and verifying from the existing state to the "erased" state, a circuit verifies the erased state after each erasing step with the "erased" state and selectively inhibits further erasing of any cells in the chunk that have been verified to have been erased correctly. This prevents over-erasing which is stressful to the device and enables efficient parallel erasing of a group of cells.

According to another aspect of the present invention, after a group of cells have been erased to the "erased" state, the cells are re-programmed to the state adjacent the "erased" state. This ensures that each erased cell starts from a well defined state, and also allows each cell to undergo similar program/erase stress.

According to another aspect of the present invention, the voltage supplied to the control gates of the EEprom cells is variable over a wide range and independent of the voltage supplied to the read circuits. This allows accurate program/erase margining as well as use in testing and diagnostics.

Additional objects, features, and advantages of the present invention will be understood from the following description of its preferred embodiments, which description should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1A** is a general micrprocessor system including the Flash EEprom memory system of the present invention;

FIG. **1B** is schematic block diagram illustrating a system including a number of Flash EEprom memory chips and a controller chip;

FIG. **2** is a schematic illustration of a system of Flash EEprom chips, among which memory sectors are selected to be erased;

FIG. **3A** is a block circuit diagram (in the controller) for implementing selective multiple sector erase according to the preferred embodiment;

FIG. **3B** shows details of a typical register used to select a sector for erase as shown in FIG. **2A**;

FIG. **4** is a flow diagram illustrating the erase sequence of selective multiple sector erase;

FIG. **5** is a schematic illustration showing the partitioning of a Flash EEprom sector into a data area and a spare redundant area;

FIG. **6** is a circuit block diagram illustrating the data path control during read operation using the defect mapping scheme of the preferred embodiment;

FIG. **7** is a circuit block diagram illustrating the data path control during the write operation using the defect mapping scheme of the preferred embodiment;

FIG. **8** is a block diagram illustrating the write cache circuit inside the controller;

FIG. **9** is a cross-sectional view of an EEprom device integrated circuit structure that can be used to implement the various aspects of the present invention;

FIG. **10** is a view of the structure of FIG. **9** taken across section **2**—**2** thereof;

FIG. **11** is an equivalent circuit of a single EEprom cell of the type illustrated in FIGS. **9** and **10**;

FIG. **12** shows an addressable array of EEprom cells;

FIG. **13** is a block diagram of an EEprom system in which the various aspects of the present invention are implemented;

FIG. **14** illustrates the partitioning of the threshold window of an EEprom cell which stores one bit of data;

FIG. **15**A illustrates the partitioning of the threshold window of an EEprom cell which stores two bits of data;

FIG. **15**B illustrates the partitioning of the source-drain conduction current threshold window of the EEprom cell of FIG. **15**A;

FIGS. **16**A and **16**B are curves that illustrate the changes and characteristics of a typical EEprom after a period of use;

FIG. **17**A illustrates read and program circuits for a master reference cell and an addressed memory cell according to the present invention;

FIG. **17**B illustrates multi-state read circuits with reference cells according to the present invention;

FIGS. **17**C(**1**)–**17**C(**8**) illustrate the timing for multi-state read for the circuits of FIG. **17**B;

FIG. **18** illustrates a specific memory organization according to the present invention;

FIG. **19** shows an algorithm for programming a set of local reference cells according to the present invention;

FIG. **20**A shows one embodiment of a read circuit using local reference cells directly;

FIG. **20**B shows a read algorithm for the embodiment of FIG. **20**A;

FIG. **21**A shows an alternative embodiment of a read circuit using local reference cells indirectly;

FIG. **21**B is a programmable circuit for the biased reading of the master reference cells according to the alternative embodiment;

FIG. **21**C is a detail circuit diagram for the programmable biasing circuit of FIG. **21**B;

FIG. **21**D shows a read algorithm for the embodiment of FIG. **21**A;

FIG. **22** illustrates the read/program data paths for a chunk of cells in parallel;

FIG. **23** shows an on chip program/verify algorithm according to the present invention;

FIG. **24** is a circuit diagram for the compare circuit according to the present invention;

FIG. **25** is a circuit diagram for the program circuit with inhibit according to the present invention; and

FIGS. **26** and **27** are tables that list typical examples of operating voltages for the EEprom cell of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

EEprom System

A computer system in which the various aspects of the present invention are incorporated is illustrated generally in FIG. **1**A. A typical computer system architecture includes a microprocessor **21** connected to a system bus **23**, along with random access, main system memory **25**, and at least one or more input-output devices **27**, such as a keyboard, monitor, modem, and the like. Another main computer system component that is connected to a typical computer system bus **23** is a large amount of long-term, non-volatile memory **29**. Typically, such a memory is a disk drive with a capacity of tens of megabytes of data storage. This data is retrieved into the system volatile memory **25** for use in current processing, and can be easily supplemented, changed or altered.

One aspect of the present invention is the substitution of a specific type of semiconductor memory system for the disk drive but without having to sacrifice non-volatility, ease of erasing and rewriting data into the memory, speed of access, low cost and reliability. This is accomplished by employing an array of electrically erasable programmable read only memories (EEprom's) integrated circuit chips. This type of memory has additional advantages of requiring less power to operate, and of being lighter in weight than a hard disk drive magnetic media memory, thereby being especially suited for battery operated portable computers.

The bulk storage memory **29** is constructed of a memory controller **31**, connected to the computer system bus **23**, and an array **33** of EEprom integrated circuit chips. Data and instructions are communicated from the controller **31** to the EEprom array **33** primarily over a serial data line **35**. Similarly, data and status signals are communicated from the EEprom **33** to the controller **31** over serial data lines **37**. Other control and status circuits between the controller **31** and the EEprom array **33** are not shown in FIG. **1**A.

Referring to FIG. **1**B, the controller **31** is preferably formed primarily on a single integrated circuit chip. It is connected to the system address and data bus **39**, part of the system bus **33**, as well as being connected to system control lines **41**, which include interrupt, read, write and other usual computer system control lines.

The EEprom array **33** includes a number of EEprom integrated circuit chips **43**, **45**, **47**, etc. Each includes a respective chip select and enable line **49**, **51** and **53** from interface circuits **40**. The interface circuits **40** also act to interface between the serial data lines **35**, **37** and a circuit **55**. Memory location addresses and data being written into or read from the EEprom chips **43**, **45**, **47**, etc. are communicated from a bus **55**, through logic and register circuits **57** and thence by another bus **59** to each of the memory chips **43**, **45**, **47** etc.

The bulk storage memory **29** of FIGS. **1**A and **1**B can be implemented on a single printed circuit card for moderate memory sizes. The various lines of the system buses **39** and **41** of FIG. **1**B are terminated in connecting pins of such a card for connection with the rest of the computer system through a connector. Also connected to the card and its components are various standard power supply voltages (not shown).

For large amounts of memory, that which is conveniently provided by a single array **33** may not be enough. In such a case, additional EEprom arrays can be connected to the serial data lines **35** and **37** of the controller chip **31**, as indicated in FIG. **1**B. This is preferably all done on a single printed circuit card but if space is not sufficient to do this, then one or more EEprom arrays may be implemented on a second printed circuit card that is physically mounted onto the first and connected to a common controller chip **31**.

Erase of Memory Structures

In system designs that store data in files or blocks the data will need to be periodically updated with revised or new information. It may also be desirable to overwrite some no longer needed information, in order to accommodate additional information. In a Flash EEprom memory, the memory cells must first be erased before information is placed in them. That is, a write (or program) operation is always preceded by an erase operation.

In conventional Flash erase memory devices, the erase operation is done in one of several ways. For example, in some devices such as the Intel corporation's model 27F-256 CMOS Flash EEprom, the entire chip is erased at one time. If not all the information in the chip is to be erased, the

information must first be temporarily saved, and is usually written into another memory (typically RAM). The information is then restored into the nonvolatile Flash erase memory by programming back into the device. This is very slow and requires extra memory as holding space.

In other devices such as Seeq Technology Incorporated's model 48512 Flash EEprom chip, the memory is divided into blocks (or sectors) that are each separately erasable, but only one at a time. By selecting the desired sector and going through the erase sequence the designated area is erased. While, the need for temporary memory is reduced, erase in various areas of the memory still requires a time consuming sequential approach.

In the present invention, the Flash EEprom memory is divided into sectors where all cells within each sector are erasable together. Each sector can be addressed separately and selected for erase. One important feature is the ability to select any combination of sectors for erase together. This will allow for a much faster system erase than by doing each one independently as in prior art.

FIG. **2** illustrates schematically selected multiple sectors for erase. A Flash EEprom system includes one or more Flash EEprom chips such as **201**, **203**, **205**. They are in communication with a controller **31** through lines **209**. Typically, the controller **31** is itself in communication with a microprocessor system (not shown). The memory in each Flash EEprom chip is partitioned into sectors where all memory cells within a sector are erasable together. For example, each sector may have 512 byte (i.e. 512×8 cells) available to the user, and a chip may have 1024 sectors. Each sector is individually addressable, and may be selected, such as sectors **211**, **213**, **215**, **217** in a multiple sector erase. As illustrated in FIG. **2**, the selected sectors may be confined to one EEprom chip or be distributed among several chips in a system. The sectors that were selected will all be erased together. This capability will allow the memory and system of the present invention to operate much faster than the prior art architectures.

FIG. **3**A illustrates a block diagram circuit **220** on a Flash EEprom chip (such as the chip **201** of FIG. **2**) with which one or more sectors such as **211**, **213** are selected (or deselected) for erase. Essentially, each sector such as **211**, **213** is selected or tagged by setting the state of an erase enable register such as **221**, **223** associated with the respective sectors. The selection and subsequent erase operations are performed under the control of the controller **31** (see FIG. **2**). The circuit **220** is in communication with the controller **31** through lines **209**. Command information from the controller is captured in the circuit **220** by a command register **225** through a serial interface **227**. It is then decoded by a command decoder **229** which outputs various control signals. Similarly, address information is captured by an address register **231** and is decoded by an address decoder **233**.

For example, in order to select the sector **211** for erase, the controller sends the address of the sector **211** to the circuit **220**. The address is decoded in line **235** and is used in combination with a set erase enable signal in bus **237** to set an output **239** of the register **221** to HIGH. This enables the sector **211** in a subsequent erase operation. Similarly, if the sector **213** is also desired to be erased, its associated register **223** may be set HIGH.

FIG. **3**B shows the structure of the register such as **221**, **223** in more detail. The erase enable register **221** is a SET/RESET latch. Its set input **241** is obtained from the set erase enable signal in bus **237** gated by the address decode in line **235**. Similarly, the reset input **243** is obtained from the clear erase enable signal in bus **237** gated by the address decode in line **235**. In this way, when the set erase enable signal or the clear erase enable signal is issued to all the sectors, the signal is effective only on the sector that is being addressed.

After all sectors intended for erase have been selected, the controller then issues to the circuit **220**, as well as all other chips in the system a global erase command in line **251** along with the high voltage for erasing in line **209**. The device will then erase all the sectors that have been selected (i.e. the sectors **211** and **213**) at one time. In addition to erasing the desired sectors within a chip, the architecture of the present system permits selection of sectors across various chips for simultaneous erase.

FIGS. **4**(**1**)–**4**(**11**) illustrate the algorithm used in conjunction with the circuit **220** of FIG. **3**A. In FIG. **4**(**1**), the controller will shift the address into the circuit **220** which is decoded in the line to the erase enable register associated with the sector that is to be erased. In FIG. **4**(**2**), the controller shifts in a command that is decoded to a set erase enable command which is used to latch the address decode signal onto the erase enable register for the addressed sector. This tags the sector for subsequent erase. In FIG. **4**(**3**), if more sectors are to be tagged, the operations described relative to FIGS. **4**(**1**)–**4**(**2**) are repeated until all sectors intended for erase have been tagged. After all sectors intended for erase have been tagged, the controller initiates an erase cycle as illustrated in FIG. **4**(**4**).

Optimized erase implementations have been disclosed in two copending U.S. patent applications. They are copending U.S. patent applications, Ser. No. 204,175, filed Jun. 8, 1988, by Dr. Eliyahou Harari, now U.S. Pat. No. 5,095,344, and one entitled "Multi-State EEprom Read and Write Circuits and Techniques," Ser. No. 07/337,579, filed Apr. 13, 1989, now abandoned, by Sanjay Mehrotra and Dr. Eliyahou Harari. The disclosures of the two applications are hereby incorporate by reference. The Flash EEprom cells are erased by applying a pulse of erasing voltage followed by a read to verify if the cells are erased to the "erased" state. If not, further pulsing and verifying are repeated until the cells are verified to be erased. By erasing in this controlled manner, the cells are not subject to over-erasure which tends to age the EEprom device prematurely as well as make the cells harder to program.

As the group of selected sectors is going through the erase cycle, some sectors will reach the "erase" state earlier than others. Another important feature of the present invention is the ability to remove those sectors that have been verified to be erased from the group of selected sectors, thereby preventing them from over-erasing.

Returning to FIG. **4**(**4**), after all sectors intended for erase have been tagged, the controller initiates an erase cycle to erase the group of tagged sectors. In FIG. **4**(**5**), the controller shifts in a global command called Enable Erase into each Flash EEprom chip that is to perform an erase. This is followed in FIG. **4**(**5**) by the controller raising of the erase voltage line (Ve) to a specified value for a specified duration. The controller will lower this voltage at the end of the erase duration time. In FIG. **4**(**6**), the controller will then do a read verify sequence on the sectors selected for erase. In FIG. **4**(**7**), if none of the sectors are verified, the sequences illustrated in FIGS. **4**(**5**)–**4**(**7**) are repeated. In FIGS. **4**(**8**) and **3**(**9**), if one or more sectors are verified to be erased, they are taken out of the sequence. Referring also to FIG. **3**A, this is achieved by having the controller address each of the verified sectors and clear the associated erase enable registers back to a LOW with a clear enable command in bus **237**.

The sequences illustrated in FIGS. **4(5)–4(10)** are repeated until all the sectors in the group are verified to be erased in FIG. **4(11)**. At the completion of the erase cycle, the controller will shift in a No Operation (NOP) command and the global Enable Erase command will be withdrawn as a protection against a false erasure.

The ability to select which sectors to erase and which ones not to, as well as which ones to stop erasing is advantageous. It will allow sectors that have erased before the slower erased sectors to be removed from the erase sequence so no further stress on the device will occur. This will increase the reliability of the system. Additional advantage is that if a sector is bad or is not used for some reason, that sector can be skipped over with no erase occurring within that sector. For example, if a sector is defective and have shorts in it, it may consume much power. A significant system advantage is gained by the present invention which allows it to be skipped on erase cycles so that it may greatly reduce the power required to erase the chip.

Another consideration in having the ability to pick the sectors to be erased within a device is the power savings to the system. The flexibility in erase configuration of the present invention enables the adaptation of the erase needs to the power capability of the system. This can be done by configuring the systems to be erased differently by software on a fixed basis between different systems. It also will allow the controller to adaptively change the amount of erasing being done by monitoring the voltage level in a system, such as a laptop computer.

An additional performance capability of the system in the present invention is the ability to issue a reset command to a Flash EEprom chip which will clear all erase enable latches and will prevent any further erase cycles from occurring. This is illustrated in FIGS. **2A** and **2B** by the reset signal in the line **261**. By doing this in a global way to all the chips, less time will be taken to reset all the erase enable registers.

An additional performance capability is to have the ability to do erase operations without regard to chip select. Once an erase is started in some of the memory chips, the controller in the system can access other memory chips and do read and write operations on them. In addition, the device(s) doing the erase can be selected and have an address loaded for the next command following the erase.

Defect Mapping

Physical defects in memory devices give rise to hard errors. Data becomes corrupted whenever it is stored in the defective cells. In conventional memory devices such as RAM's and Disks, any physical defects arising from the manufacturing process are corrected at the factory. In RAM's, spare redundant memory cells on chip may be patched on, in place of the defective cells. In the traditional disk drive, the medium is imperfect and susceptible to defects. To overcome this problem manufacturers have devised various methods of operating with these defects present, the most usual being defect mapping of sectors. In a normal disk system the media is divided into cylinders and sectors. The sector being the basic unit in which data is stored. When a system is partitioned into the various sectors the sectors containing the defects are identified and are marked as bad and not to be used by the system. This is done in several ways. A defect map table is stored on a particular portion of the disk to be used by the interfacing controller. In addition, the bad sectors are marked as bad by special ID and flag markers. When the defect is addressed, the data that would normally be stored there is placed in an alternative location. The requirement for alternative sectors makes the system assign spare sectors at some specific interval or location. This reduces the amount of memory capacity and is a performance issue in how the alternative sectors are located.

One important application of the present invention is to replace a conventional disk storage device with a system incorporating an array of Flash EEprom memory chips. The EEprom system is preferably set up to emulate a conventional disk, and may be regarded as a "solid-state disk".

In a "disk" system made from such solid-state memory devices, low cost considerations necessitate efficient handling of defects. Another important feature of the invention enables the error correction scheme to conserve as much memory as possible. Essentially, it calls for the defective cells to be remapped cell by cell rather than by throwing away the whole sector (512 bytes typically) whenever a defect occurs in it. This scheme is especially suited to the Flash EEprom medium since the majority of errors will be bit errors rather than a long stream of adjacent defects as is typical in traditional disk medium.

In both cases of the prior art RAM and magnetic disk, once the device is shipped from the factory, there is little or no provision for replacing hard errors resulting from physical defects that appear later during normal operation. Error corrections then mainly rely on schemes using error correction codes (ECC).

The nature of the Flash EEprom device predicates a higher rate of cell failure especially with increasing program/erase cycling. The hard errors that accumulate with use would eventually overwhelm the ECC and render the device unusable. One important feature of the present invention is the ability for the system to correct for hard errors whenever they occur. Defective cells are detected by their failure to program or erase correctly. Also during read operation, defective cells are detected and located by the ECC. As soon as a defective cell is identified, the controller will apply defect mapping to replace the defective cell with a space cell located usually within the same sector. This dynamic correction of hard errors, in addition to conventional error correction schemes, significantly prolongs the life of the device.

Another feature of the present invention is an adaptive approach to error correction. Error correction code (ECC) is employed at all times to correct for soft errors as well as any hard errors that may arise. As soon as a hard error is detected, defect mapping is used to replace the defective cell with a spare cell in the same sector block. Only when the number of defective cells in a sector exceeds the defect mapping's capacity for that specific sector will the whole sector be replaced as in a conventional disk system. This scheme minimized wastage without compromising reliability.

FIG. **5** illustrates the memory architecture for the cell remapping scheme. As described before, the Flash EEprom memory is organized into sectors where the cells in each sector are erasable together. The memory architecture has a typical sector **401** organized into a data portion **403** and a spare (or shadow) portion **405**. The data portion **403** is memory space available to the user. The spare portion **405** is further organized into an alternative defects data area **407**, a defect map area **409**, a header area **411** and an ECC and others area **413**. These areas contain information that could be used by the controller to handle the defects and other overhead information such as headers and ECC.

Whenever a defective cell is detected in the sector, a good cell in the alternative defects data area **407** is assigned to backup the data designated for the defective cell. Thus even

if the defective cell stores the data incorrectly, an error-free copy is stored in the backup cell. The addresses of the defective cell and the backup cell are stored as defect pointers in the defect map **409**.

It is to be understood that the partitioning between the user data portion **403** and the spare portion **405** need not be rigid. The relative size of the various partitioned areas may be logically reassigned. Also the grouping of the various areas is largely for the purpose of discussion and not necessarily physically so. For example, the alternative defects data area **407** has been schematically grouped under the spare portion **405** to express the point that the space it occupies is no longer available to the user.

In a read operation, the controller first reads the header, the defect map and the alternative defects data. It then reads the actual data. It keeps track of defective cells and the location of the substitute data by means of the defect map. Whenever a defective cell is encountered, the controller substitutes its bad data with the good data from the alternative defects.

FIG. **6** illustrates the read data path control in the preferred embodiment. A memory device **33** which may include a plurality of Flash EEprom chips is under the control of the controller **31**. The controller **31** is itself part of a microcomputer system under the control of a microprocessor (not shown). To initiate the reading of a sector, the microprocessor loads a memory address generator **503** in the controller with a memory address for starting the read operation. This information is loaded through a microprocessor interface port **505**. Then the microprocessor loads a DMA controller **507** with the starting location in buffer memory or bus address that the data read should be sent. Then the microprocessor loads the header information (Head, Cylinder and sector) into a holding register file **509**. Finally, the microprocessor loads a command sequencer **511** with a read command before passing control to the controller **31**.

After assuming control, the controller **31** first addresses the header of the sector and verifies that the memory is accessed at the address that the user had specified. This is achieved by the following sequence. The controller selects a memory chip (chip select) among the memory device **33** and shifts the address for the header area from the address generator **503** out to the selected memory chip in the memory device **33**. The controller then switches the multiplexer **513** and shifts also the read command out to the memory device **33**. Then the memory device reads the address sent it and begins sending serial data from the addressed sector back to the controller. A receiver **515** in the controller receives this data and puts it in parallel format. In one embodiment, once a byte (8 bits) is compiled, the controller compares the received data against the header data previously stored by the microprocessor in the holding register file **509**. If the compare is correct, the proper location is verified and the sequence continues.

Next the controller **31** reads the defect pointers and loads these bad address locations into the holding register file **509**. This is followed by the controller reading the alternative defects data that were written to replace the bad bits as they were written. The alternative bits are stored in an alternative defects data file **517** that will be accessed as the data bits are read.

Once the Header has been determined to be a match and the defect pointers and alternative bits have been loaded, the controller begins to shift out the address of the lowest address of the desired sector to be read. The data from the sector in the memory device **33** is then shifted into the controller chip **31**. The receiver **515** converts the data to a parallel format and transfers each byte into a temporary holding FIFO **519** to be shipped out of the controller.

A pipeline architecture is employed to provide efficient throughput as the data is gated through the controller from the receiver **515** to the FIFO **519**. As each data bit is received from memory the controller is comparing the address of the data being sent (stored in the address generator **507**) against the defect pointer map (stored in the register file **509**). If the address is determined to be a bad location, by a match at the output of the comparator **521**, the bad bit from the memory received by the receiver **515** is replaced by the good bit for that location. The good bit is obtained from the alternative defects data file **517**. This is done by switching the multiplexer **523** to receive the good bit from the alternative defects data file instead of the bad bit from the receiver **515**, as the data is sent to the FIFO **519**. Once the corrected data is in the FIFO it is ready to be sent to buffer memory or system memory (not shown). The data is sent from the controller's FIFO **519** to the system memory by the controller's DMA controller **507**. This controller **507** then requests and gets access to the system bus and puts out an address and gates the data via an output interface **525** out to the system bus. This is done as each byte gets loaded into the FIFO **519**. As the corrected data is loaded into the FIFO it will also be gated into an ECC hardware **527** where the data file will be acted on by the ECC.

Thus in the manner described, the data read from the memory device **33** is gated through the controller **31** to be sent to the system. This process continues until the last bit of addressed data has been transferred.

In spite of defect mapping of previously detected defective cells, new hard errors might occur since the last mapping. As the dynamic defect mapping constantly "puts away" new defective cells, the latest hard error that may arise between defect mapping would be adequately handled by the ECC. As the data is gated through the controller **31**, the controller is gating the ECC bits into the ECC hardware **527** to determine if the stored value matched the just calculated remainder value. If it matches then the data transferred out to the system memory was good and the read operation was completed. However, if the ECC registers an error then a correction calculation on the data sent to system memory is performed and the corrected data retransmitted. The method for calculating the error can be done in hardware or software by conventional methods. The ECC is also able to calculate and locate the defective cell causing the error. This may be used by the controller **31** to update the defect map associated with the sector in which the defective cell is detected. In this manner, hard errors are constantly removed from the Flash EEprom system.

FIG. **7** illustrates the write data path control in the preferred embodiment. The first portion of a write sequence is similar to a read sequence described previously. The microprocessor first loads the Address pointers for the memory device **33** and the DMA as in the read sequence. It also loads the header desired into the address generator **503** and the command queue into the command sequencer **511**. The command queue is loaded with a read header command first. Thereafter, control is passed over to the controller **31**. The controller then gates the address and command to the memory device **33**, as in the read sequence. The memory device returns header data through controller's receiver **515**. The controller compares the received header data to the expected value (stored in the holding register file **509**). If the compare is correct, the proper location is verified and the sequence continues. Then the controller loads the defective address pointers from the memory device **33** into the holding

register file **509** and the alternative data into the alternative defects data file **517**.

Next, the controller begins to fetch the write data from system memory (not shown). It does this by getting access to the system bus, outputs the memory or bus address and does the read cycle. It pulls the data into a FIFO **601** through an input interface **603**. The controller then shifts the starting sector address (lowest byte address) from the address generator **503** to the selected memory device **33**. This is followed by data from the FIFO **601**. These data are routed through multiplexers **605** and **513** and converted to serial format before being sent to the memory device **33**. This sequence continues until all bytes for a write cycle have been loaded into the selected memory.

A pipeline architecture is employed to provide efficient throughput as the data is gated from the FIFO **601** to the selected memory **33**. The data gated out of the FIFO **601** is sent to the ECC hardware **527** where a remainder value will be calculated within the ECC. In the next stage, as the data is being sent to the memory device through multiplexers **605** and **513**, the comparator **521** is comparing its address from the address generator **503** to the defect pointer address values in the holding register file **509**. When a match occurs, indicating that a defective location is about to be written, the controller saves this bit into the alternative defect data file **517**. At the same time, all bad bits sent to memory will be sent as zeroes.

After the bytes for a write cycle have been loaded into the selected memory device, the controller issues a program command to the memory device and initiate a write cycle. Optimized implementations of write operation for Flash EEprom device have been disclosed in two previously cited co-pending U.S. patent applications, Ser. No. 204,175, now U.S. Pat. No. 5,095,344 and one entitled "Multi-State EEprom Read and Write Circuits and Techniques, Ser. No. 07/337,579, filed Apr. 13, 1989, now abandoned." Relevant portions of the disclosures are hereby incorporated by reference. Briefly, during the write cycle, the controller applies a pulse of programming (or writing) voltages. This is followed by a verify read to determine if all the bits have been programmed properly. If the bits did not verify, the controller repeats the program/verify cycle until all bits are correctly programmed.

If a bit fails to verify after prolonged program/verify cycling, the controller will designate that bit as defective and update the defect map accordingly. The updating is done dynamically, as soon as the defective cell is detected. Similar actions are taken in the case of failure in erase verify.

After all the bits have been programmed and verified, the controller loads the next data bits from the FIFO **601** and addresses the next location in the addressed sector. It then performs another program/verify sequence on the next set of bytes. The sequence continues until the end of the data for that sector. Once this has occurred, the controller addresses the shadow memory (header area) associated with the sector (see FIG. **5**) and writes the contents of the ECC registers into this area.

In addition, the collection of bits that was flagged as defective and were saved in the alternative defects data file **516** is then written in memory at the alternative defects data locations (see FIG. **5**), thereby saving the good bit values to be used on a subsequent read. Once these data groups are written and verified, the sector write is considered completed.

The present invention also has provision for defect mapping of the whole sector, but only after the number of defective cells in the sector has exceeded the cell defect mapping's capacity for that specific sector. A count is kept of the number of defective cells in each sector. When the number in a sector exceeds a predetermined value, the controller marks that sector as defective and maps it to another sector. The defect pointer for the linked sectors may be stored in a sector defect map. The sector defect map may be located in the original defective sector if its spare area is sufficiently defect-free. However, when the data area of the sector has accumulated a large number of defects, it is quite likely that the spare area will also be full of defects.

Thus, it is preferable in another embodiment to locate the sector map in another memory maintained by the controller. The memory may be located in the controller hardware or be part of the Flash EEprom memory. When the controller is given an address to access data, the controller compares this address against the sector defect map. If a match occurs then access to the defective sector is denied and the substitute address present in the defect map is entered, and the corresponding substitute sector is accessed instead.

In yet another embodiment, the sector remapping is performed by the microprocessor. The microprocessor looks at the incoming address and compares it against the sector defect map. If a match occurs, it does not issue the command to the controller but instead substitute the alternative location as the new command.

Apart from the much higher speed of the solid-state disk, another advantage is the lack of mechanical parts. The long seek times, rotational latency inherent in disk drives are not present. In addition, the long synchronization times, sync mark detects and write gaps are not required. Thus the overhead needed for accessing the location where data is to be read or written is much less. All of these simplifications and lack of constraints result in a much faster system with much reduced overheads. In addition, the files can be arranged in memory in any address order desired, only requiring the controller to know how to get at the data as needed.

Another feature of the invention is that defect mapping is implemented without the need to interrupt the data stream transferred to or from the sector. The data in a block which may contain errors are transferred regardless, and is corrected afterwards. Preserving the sequential addressing will result in higher speed by itself. Further, it allows the implementation of an efficient pipeline architecture in the read and write data paths.

Write Cache System

Cache memory is generally used to speed up the performance of systems having slower access devices For example in a computer system, access of data from disk storage is slow and the speed would be greatly improved if the data could be obtained from the much faster RAM. Typically a part of system RAM is used as a cache for temporarily holding the most recently accessed data from disk. The next time the data is needed, it may be obtained from the fast cache instead of the slow disk. The scheme works well in situations where the same data is repeatedly operated on. This is the case in most structures and programs since the computer tends to work within a small area of memory at a time in running a program. Another example of caching is the using of faster SRAM cache to speed up access of data normally stored in cheaper but slower DRAM.

Most of the conventional cache designs are read caches for speeding up reads from memory. In some cases, write caches are used for speeding up writes to memory. However in the case of writes to system memory (e.g. disks), data is still being written to system memory directly every time they occur, while being written into cache at the same time.

This is done because of concern for loss of updated data files in case of power loss. If the write data is only stored in the cache memory (volatile) a loss of power will result in the new updated files being lost from cache before having the old data updated in system memory (non-volatile). The system will then be operating on the old data when these files are used in further processing. The need to write to main memory every time defeats the caching mechanism for writes. Read caching does not have this concern since the data that could be lost from cache has a backup on disk.

In the present invention, a system of Flash EEprom is used to provide non-volatile memory in place of traditional system memories such as disk storage. However, Flash EEprom memory is subject to wearing out by excessive program/erase cycles. Even with the improved Flash EEprom memory device as disclosed in co-pending U.S. patent applications, Ser. No. 204,175, now U.S. Pat. No. 5,095,244, and one intitled "multi-state EEprom Read and Write Circuits and Techniques," by sanjay Mehrotra and Dr. Eliyahou Harari, Ser. No. 07/337,579, filed Apr. 13, 1989, now abandoned, the endurance limit is approximately 10^6 program/erase cycles. In a ten-year projected life time of the device, this translates to a limit of one program/erase cycle per 5 minutes. This may be marginal in normal computer usage.

To overcome this problem, a cache memory is used in a novel way to insulate the Flash EEprom memory device from enduring too many program/erase cycles. The primary function of the cache is to act on writes to the Flash EEprom memory and not on reads of the Flash EEprom memory, unlike the case with traditional caches. Instead of writing to the Flash EEprom memory every time the data is updated, the data may be operated on several times in the cache before being committed to the Flash EEprom memory. This reduces the number of writes to the Flash EEprom memory. Also, by writing mostly into the faster cache memory and reducing the number of writes to the slower Flash EEprom, an additional benefit is the increase in system write throughput.

A relatively small size cache memory is quite effective to implement the present invention. This helps to overcome the problem of data loss in the volatile cache memory during a power loss. In that event, it is relatively easy to have sufficient power reserve to maintain the cache memory long enough and have the data dumped into a non-volatile memory such as a specially reserved space in the Flash EEprom memory. In the event of a power down or and power loss to the system, the write cache system may be isolated from the system and a dedicated rechargeable power supply may be switch in only to power the cache system and the reserved space in the Flash EEprom memory.

FIG. **8** illustrates schematically a cache system **701** as part of the controller, according to the present invention. On one hand the cache system **701** is connected to the Flash EEprom memory array **33**. On the other hand it is connected to the microprocessor system (not shown) through a host interface **703**. The cache system **701** has two memories. One is a cache memory **705** for temporarily holding write data files. The other is a tag memory **709** for storing relevant information about the data files held in the cache memory **705** A memory timing/control circuit **713** controls the writing of data files from the cache memory **705** to the Flash EEprom memory **33**. The memory control circuit **713** is responsive to the information stored in the tag memory as well as a power sensing input **715** with is connected through the host interface **703** via a line **717** to the power supply of the microprocessor system. A power loss in the microprocessor system will be sensed by the memory control circuit **713** which will then down load all the data files in the volatile cache memory **705** to the non-volatile Flash EEprom memory **33**.

In the present invention, the Flash EEprom memory array **33** is organized into sectors (typically 512 byte size) such that all memory cells within each sector are erasable together. Thus each sector may be considered to store a data file and a write operation on the memory array acts on one or more such files.

During read of a new sector in the Flash EEprom memory **33**, the data file is read out and sent directly to the host through the controller. This file is not used to fill the cache memory **705** as is done in the traditional cache systems.

After the host system has processed the data within a file and wishes to write it back to the Flash EEprom memory **33**, it accesses the cache system **701** with a write cycle request. The controller then intercepts this request and acts on the cycle.

In one embodiment of the invention, the data file is written to the cache memory **705**. At the same time, two other pieces of information about the data file are written to a tag memory **709**. The first is a file pointer which identifies the file present in the cache memory **705**. The second is a time stamp that tells what time the file was last written into the cache memory. In this way, each time the host wishes to write to the Flash EEprom memory **33**, the data file is actually first stored in the cache memory **705** along with pointers and time stamps in the tag memory **709**.

In another embodiment of the invention, when a write from the host occurs, the controller first checks to see if that file already existed in the cache memory **705** or has been tagged in the tag memory **709**. If it has not been tagged, the file is written to the Flash memory **33**, while its identifier and time stamp are written to the tag memory **709**. If the file already is present in the cache memory or has been tagged, it is updated in the cache memory and not written to the Flash memory. In this way only infrequently used data files are written into the Flash memory while frequently used data files are trapped in the cache memory.

In yet another embodiment of the invention, when a write from the host occurs, the controller first checks to see if that data file has been last written anywhere within a predetermined period of time (for example, 5 minutes). If it has not, the data file is written to the Flash memory **33**, while its identifier and time stamp are written to the tag memory **709**. If the data file has been last written within the predetermined period of time, it is written into the cache memory **705** and not written to the Flash memory. At the same time, its identifier and time stamp are written to the tag memory **709** as in the other embodiments. In this way also, only infrequently used data files are written into the Flash memory while frequently used data files are trapped in the cache memory.

In all embodiments, over time the cache memory **705** will start to fill up. When the controller has detected that some predetermined state of fullness has been reached, it begins to archive preferentially some files over others in the cache memory **705** by writing them to the Flash memory **33**.

In either embodiments, over time the cache memory **705** will start to fill up. When the controller has detected that some predetermined state of fullness has been reached, it begins to archive preferentially some files over others in the cache memory **705** by writing them to the Flash memory **33**. The file identifier tag bits for these files are then reset, indicating that these files may be written over. This makes room for new data files entering the cache memory.

The controller is responsible for first moving the least active files back into the Flash memory **33** to make room for

new active files. To keep track of each file's activity level, the time stamp for each file is incremented by the controller at every time step unless reset by a new activity of the file. The timing is provided by timers **711**. At every time step (count), the controller systematically accesses each data file in the cache memory and reads the last time stamp written for this data file. The controller then increments the time stamp by another time step (i.e. increments the count by one).

Two things can happen to a file's time stamp, depending on the activity of the file. One possibility is for the time stamp to be reset in the event of a new activity occurring. The other possibility is that no new activity occurs for the file and the time stamp continues to increment until the file is removed from the cache. In practice a maximum limit may be reached if the time stamp is allowed to increase indefinitely. For example, the system may allow the time stamp to increment to a maximum period of inactivity of 5 minutes. Thus, when a data file is written in the cache memory, the time stamp for the file is set at its initial value. Then the time stamp will start to age, incrementing at every time step unless reset to its initial value again by another write update. After say, 5 minutes of inactivity, the time stamp has incremented to a maximum terminal count.

In one embodiment of keeping count, a bit can be shifted one place in a shift register each time a count increment for a file occurs. If the file is updated (a new activity has occurred) the bit's location will be reset to the initial location of the shift register. On the other hand, if the file remains inactive the bit will eventually be shifted to the terminal shift position. In another embodiment, a count value for each file is stored and incremented at each time step. After each increment, the count value is compared to a master counter, the difference being the time delay in question.

Thus, if a file is active its incremented time stamp is reset back to the initial value each time the data file is rewritten. In this manner, files that are constantly updated will have low time stamp identifiers and will be kept in cache until their activity decreases. After a period of inactivity has expired, they acquire the maximum time stamp identifiers. The inactive files are eventually archived to the Flash memory freeing space in the cache memory for new, more active files. Space is also freed up in the tag memory when these inactive files are moved to the Flash memory.

At any time when room must be made available for new data files coming into the cache memory, the controller removes some of the older files and archives them to the Flash memory **33**. Scheduling is done by a memory timing/control circuit **713** in the controller. The decision to archive the file is based on several criteria. The controller looks at the frequency of writes occurring in the system and looks at how full the cache is. If there is still room in the cache, no archiving need to be done. If more room is needed, the files with the earliest time stamps are first removed and archived to the Flash memory.

Although the invention has been described with implementation in hardware in the controller, it is to be understood that other implementations are possible. For example, the cache system may be located elsewhere in the system, or be implemented by software using the existing microprocessor system. Such variations are within the scope of protection for the present invention.

The Profile of how often data is written back to the Flash memory is determined by several factors. It depends on the size of the cache memory and the frequency of writes occurring in the system. With a small cache memory system, only the highest frequency files will be cached. Less frequently accessed files will also be cached with increasing cache memory size. In the present invention, a relatively cheap and small amount of cache memory, preferably about 1 Mbyte, may be used to good advantage. By not constantly writing the most active files (the top 5%), the write frequency of the Flash EEprom may be reduced from the usual one every millisecond to one every 5 minutes. In this way the wear-out time for the memory can be extended almost indefinitely. This improvement is also accompanied by increased system performance during write.

Incorporating time tag into the write cache concept has the advantage that the size of the write cache buffer memory can be relatively small, since it is used only to store frequently written data files, with all other files written directly into the Flash EEprom memory. A second advantage is that the management of moving data files in and out of the write cache buffer can be automated since it does not require advanced knowledge of which data files are to be called next.

The various aspects of the present invention that have been described co-operate in a system of Flash EEprom memory array to make the Flash EEprom memory a viable alternative to conventional non-volatile mass storage devices.

There are many specific Eprom, EEprom semiconductor integrated circuit structures that can be utilized in making a memory array with which the various aspects of the present invention are advantageously implemented.

"Split-Channel" EEprom Cell

A preferred EEprom structure is generally illustrated in the integrated circuit cross-sectional views of FIGS. **9** and **10**. Describing this preferred structure briefly, two memory cells **1011** and **1013** are formed on a lightly p-doped substrate **1015**. A heavily n-doped implanted region **1017** between the cells **1011** and **1013** serves as a drain for the cell **1011** and a source for the cell **1013**. Similarly, another implanted n-doped region **1019** is the source of the cell **1011** and the drain of an adjacent cell, and similarly for another n-doped region **1021**.

Each of the memory cells **1011** and **1013** contains respective conductive floating gates **1023** and **1025**, generally made of polysilicon material. Each of these floating gates is surrounded by dielectric material so as to be insulated from each other and any other conductive elements of the structure. A control gate **1027** extends across both of the cells **1011** and **1013** in a manner to be insulated from the floating gates and the substrate itself. As shown in FIG. **10**, conductive strips **1029** and **1031** are additionally provided to be insulated from each other and other conductive elements of the structure, serving as erase gates. A pair of such erase gates surrounds the floating gate of each memory cell and are separated from it by an erase dielectric layer. The cells are isolated by thick field oxide regions, such as regions **1033**, **1035**, and **1037**, shown in the cross-section of FIG. **9**, and regions **1039** and **1041** shown in the view of FIG. **10**.

The memory cell is programmed by transferring electrons from the substrate **1015** to a floating gate, such as the floating gate **1025** of the memory cell **1013**. The charge on the floating gate **1025** is increased by electrons travelling across the dielectric from a heavily p-doped region **1043** and onto the floating gate. Charge is removed from the floating gate through the dielectric between it and the erase gates **1029** and **1031**. This preferred EEprom structure, and a process for manufacturing it, are described in detail in copending patent application Ser. No. 323,779 of Jack H. Yuan and Eliyahou Harari, filed Mar. 15, 1989, which is expressly incorporated herein by reference.

The EEprom structure illustrated in FIGS. **9** and **10** is a "split-channel" type. Each cell may be viewed as a composite transistor consisting of two transistor T1 and T2 in series as shown in FIG. **11**. The T1 transistor **1011***a* is formed along the length L1 of the channel of the cell **1011** of FIG. **9**. It has a variable threshold voltage V_{T1}. In series with the T1 transistor **1011***a* is the T2 transistor **1011**b that is formed in a portion of the channel L2. It has a fixed threshold voltage VT_2 of about 1 V. Elements of the equivalent circuit of FIG. **11** are labeled with the same reference numbers as used for corresponding parts in FIGS. **9** and **10**, with a prime (') added.

As can best be seen from the equivalent circuit of FIG. **11**, the level of charge on the T1's floating gate **1023**' of an EEprom cell affects the threshold voltage V_{T1} of the T1 transistor **1011***a* when operated with the control gate **1027**'. Thus, a number of memory states may be defined in a cell, corresponding to well defined threshold voltages programmed into the cell by an appropriate amount of charge placed on the floating gate. The programming is performed by applying, over a certain period of time, appropriate voltages to the cell's control gate **1027**' as well as drain **1017**' and source **1019**'.

Addressable Flash EEprom Array

The various aspects of the present invention are typically applied to an array of Flash EEprom cells in an integrated circuit chip. FIG. **12** illustrates schematically an array of individually addressable EEprom cells **1060**. Each cell is equivalent to the one shown in FIG. **11**, having a control gate, source and drain, and an erase gate. The plurality of individual memory cells are organized in rows and columns. Each cell is addressed by selectively energizing its row and column simultaneously. A column **1062**, for example, includes a first memory cell **1063**, an adjacent second memory cell **1065**, and so forth. A second column **1072** includes memory cells **1073**, **1075**, and so forth. Cells **1063** and **1073** are located in a row **1076**, cells **1065** and **1071** in another, adjacent row, and so forth.

Along each row, a word line is connected to all the control gates of the cells in the row. For example, the row **1076** has the word line **1077** and the next row has the word line **1079**. A row decoder **1081** selectively connects the control gate voltage VCG on an input line **1083** to all the control gates along a selected word line for a row.

Along each column, all the cells have their sources connected by a source line such as **1091** and all their drains by a drain line such as **1093**. Since the cells along a row are connected in series by their sources and drains, the drain of one cell is also the source of the adjacent cell. Thus, the line **1093** is the drain line for the column **1062** as well as the source line for the column **1072**. A column decoder **1101** selectively connects the source voltage V_S on an input line **1103** to all the sources and connects the drain voltage V_D on an input line **1105** to all the drains along a selected column.

Each cell is addressed by the row and column in which it is located. For example, if the cell **1075** is addressed for programming or reading, appropriate programming or reading voltages must be supplied to the cell's control gate, source and drain. An address on the internal address bus **1111** is used to decode row decoder **1081** for connecting V_{CG} to the word line **1079** connected to the control gate of the cell **1075**. The same address is used to decode column decoder **1101** for connecting V_S to the source line **1093** and V_D to the drain line **1095**, which are respectively connected to the source and drain of the cell **1075**.

One aspect of the present invention, which will be disclosed in more detail in a later section, is the implementation of programming and reading of a plurality of memory cells in parallel. In order to select a plurality of columns simultaneously, the column decoder, in turn, controls the switching of a source multiplexer **1107** and a drain multiplexer **1109**. In this way, the selected plurality of columns may have their source lines and drain lines made accessible for connection to V_S and V_D respectively.

Access to the erase gate of each cell is similar to that of the control gate. In one implementation, an erase line such as **1113** or **1115** or **1117** is connected to the erase gate of each cells in a row. An erase decoder **1119** decodes an address on the internal address bus **1111** and selectively connects the erase voltage V_{EG} on input line **1121** to an erase line. This allows each row of cells to be addressed independently, such as the row **1076** being simultaneously (Flash) erased by proper voltages applied to their erase gates through erase line **1113**. In this case, the Flash cell consists of one row of memory cells. However, other Flash cell's implementations are possible and most applications will provide for simultaneous erasing of many rows of cells at one time.

Flash EEprom System

The addressable EEprom array **1060** in FIG. **12** forms part of the larger multi-state Flash EEprom system of the present invention as illustrated in FIG. **13**. In the larger system, an EEprom integrated circuit chip **1130** is controlled by a controller **1140** via an interface **1150**. The controller **1140** is itself in communication with a central microprocessor unit **1160**.

The EEprom chip **1130** comprises the addressable EEprom array **1060**, a serial protocol logic **1170**, local power control circuits **1180**, and various programming and reading circuits **1190**, **1200**, **1210**, **1220**, **1230** and **1240**.

The controller **1140** controls the functioning of the EEprom chip **1130** by supplying the appropriate voltages, controls and timing. Tables of FIGS. **26** and **27** show typical examples of voltage conditions for the various operational modes of the EEprom cell. The addressable EEprom array **1060** may be directly powered by the controller **1140** or, as shown in FIG. **13**, be further regulated on chip by the local power control **1180**. Control and data linkages between the controller **1140** and the chip **1130** are made through the serial in line **1251** and the serial out line **1253**. Clock timing is provided by the controller via line **1255**.

In a typical operation of the EEprom chip **1130**, the controller **1140** will send a serial stream of signals to the chip **1130** via serial in line **1251**. The signals, containing control, data, address and timing information, will be sorted out by the serial protocol logic **1170**. In appropriate time sequence, the logic **1170** outputs various control signals **1257** to control the various circuits on the chip **1130**. It also sends an address via the internal address bus **111** to connect the addressed cell to voltages put out from the controller. In the meantime, if the operation is programming, the data is staged for programming the addressed cell by being sent via a serial data line **1259** to a set of read/program latches and shift registers **1190**.

Read Circuits and Techniques Using Reference Cells

To accurately and reliably determine the memory state of a cell is essential for EEprom operations. This is because all the basic functions such as read, erase verify and program verify depend on it. Improved and novel read circuits **1220** for the EEprom chip **1130** and techniques of the present invention make multi-state EEprom feasible.

As discussed in connection with FIG. **11**, the programmed charge placed on the floating gate **1023**' determines the programmed threshold voltage V_{T1} of the cell. Generally, V_{T1} increases or decreases with the amount of negative

charge on the floating gate **1023**'. The charge can even be reduced to a positive value (depletion mode) where V_{T1} decreases below VT_2 and even becomes negative. The maximum and minimum values of V_{T1} are governed by the dielectric strength of the device material. The span of V_{T1} defines a threshold voltage window in which memory states may be implemented.

Copending patent application Ser. No. 204,175, now U.S. Pat. No. 5,095,344 discloses an EEprom cell with memory states defined within a maximized window of threshold voltage V_{T1}. The full threshold voltage window includes the negative region of the threshold voltage, in addition to the usual positive region. The increased window provides more memory space to implement multi-state in an EEprom cell.

FIGS. **14** and **15** respectively illustrate the manner in which the threshold voltage window is partitioned for a 2-state memory and a 4-state memory cell. (of course it is also possible to partition the window for a 3-state memory or even for a continuum of states in an analog, rather than digital memory).

Referring first to FIG. **14**, the solid curve **1343** shows V_{T1} as a function of programming time. The threshold voltage window is delimited by the minimum and maximum values of V_{T1}, represented approximately by the Erase state level **1345** and the Fully Program state level **1347** respectively. The 2-state memory is implemented by partitioning the window into two halves **1346**, **1348** using a breakpoint threshold level **1349**. Thus, the cell may be considered to be in memory state 0 (or state 1) if the cell is programmed with a V_{T1} within region **1346** (or region **1348**) respectively.

A typical erase/program cycle begins with erase which reduces the threshold voltage of the cell to its Erase state level **1345**. Subsequent repetitive programming is used to increase the threshold voltage V_{T1} to the desired level. Rather than continuously applying programming voltages to the addressed cell for some fixed period of time corresponding to the state to which the cell is to be programmed, it is preferable to apply programming voltages in repetitive short pulses with a read operation occurring after each pulse to determine when it has been programmed to the desired threshold voltage level, at which time the programming terminates. The programming voltages and duration of the pulses are such that the pulses advance V_{T1} across the various regions rapidly but each pulse is sufficiently fine to not overshoot any of the regions. This minimizes voltage and field related stresses on the cell, and therefore improves its reliability.

FIG. **15**A illustrates the 4-state case where the threshold voltage window is partitioned into four regions **1351**, **1353**, **1355**, **1357** by breakpoint levels **1352**, **1354**, **1356** respectively. The cell is considered to be in state "3" or "2" or "1" or "0" if its V_{T1} is programmed to be within corresponding regions **1351** or **1353** or **1355** or **1357** respectively. A 4-state cell is able to store two bits of data. Thus, the four states may be encoded as (1,1), (1,0), (0,1) and (0,0) respectively.

In general, if each EEprom cell is to store K states, the threshold window must be partitioned into K regions with at least K−1 threshold levels. Thus, only one breakpoint level is required for a 2-state memory cell, and three breakpoint levels are required for a 4-state cell.

In principle, a threshold voltage window may be partitioned to a large number of memory states. For example, for an EEprom device with a maximum threshold window of 16 V, it may be partitioned into thirty-two states each within an approximately half volt interval. In practice, prior art EEprom devices have only stored two states or one bit per cell with diminished reliability and life. Apart from operating with a smaller threshold window, prior devices fail to solve two other problems inherent in EEprom devices. Both problems relate to the uncertainty in the amount of charge in the floating gate and hence the uncertainty in the threshold voltage VT1 programmed into the cell.

The first problem has to do with the endurance-related stress the device suffers each time it goes through an erase/program cycle. The endurance of a Flash EEprom device is its ability to withstand a given number of program/erase cycles. The physical phenomenon limiting the endurance of prior art Flash EEprom devices is trapping of electrons in the active dielectric films of the device. During programming, electrons are injected from the substrate to the floating gate through a dielectric interface. Similarly, during erasing, electrons are extracted from the floating gate to the erase gate through a dielectric interface. In both cases, some of the electrons are trapped by the dielectric interface. The trapped electrons oppose the applied electric field in subsequent program/erase cycles thereby causing the programmed V_{T1} to shift to a lower value and the erased V_{T1} to shift to a higher value. This can be seen in a gradual closure in the voltage "window" between the "0" and "1" states of prior art devices as shown in FIG. **16**A. Beyond approximately 1×10^4 program/erase cycles the window closure can become sufficiently severe to cause the reading circuitry to malfunction. If cycling is continued, the device eventually experiences catastrophic failure due to a ruptured dielectric. This typically occurs at between 1×10^6 and 1×10^7 cycles, and is known as the intrinsic breakdown of the device. In prior art EEprom devices the window closure is what limits the practical endurance to approximately 1×10^4 program/erase cycles. This problem is even more critical if multi-state memory is implemented, since more accurate placement of V_{T1} is demanded.

A second problem has to do with the charge retention on the floating gate. The charge on the floating gate tends to diminish somewhat through leakage over a period of time. This causes the threshold voltage V_{T1} to shift also to a lower value over time. FIG. **16**B illustrates the reduction of V_{T1} as a function of time. Over the life time of the device V_{T1} may shift by as much as 1 V. In a multi-state device, this could shift the memory by one or two states.

The present invention overcomes these problems and presents circuits and techniques to reliably program and read the various states even in a multi-state implementation. The memory state of a cell may be determined by measuring the threshold voltage V_{T1} programmed therein. Alternatively, as set forth in copending patent application, Ser. No. 204,175, now U.S. Pat. No. 5,094,344, the memory state may conveniently be determined by measuring the differing conduction in the source-drain current I_{DS} for the different states. In the 4-state example, FIG. **15**A shows the partition in the threshold voltage window. FIG. **15**B, on the other hand, illustrates typical values of I_{DS} (solid curves) for the four states as a function of the control gate voltage V_{CG}. With V_{CG} at 5 V, the I_{DS} values for each of the four conduction states can be distinguished by sensing with four corresponding current sensing amplifiers in parallel. Associated with each amplifier is a corresponding reference conduction states IREF level (shown as broken curves in FIG. **16**). Just as the breakpoint threshold levels (see FIGS. **14** and **15**A) are used to demarcate the different regions in the threshold voltage window, the I_{REF} levels are used to do the same in the corresponding source-drain current window. By comparing with the I_{REF}'S. the conduction state of the memory cell can be determined. Co-pending patent application, Ser. No. 204,175 proposes using the same sensing amplifiers and

I_{REF}'S for both programming and reading. This provides good tracking between the reference levels (broken curves in FIG. **15**B) and the programmed levels (solid curves in FIG. **15**B).

In the improved scheme of the present invention, the I_{REF}'S are themselves provided by the source-drain currents of a set of EEprom cells existing on the same chip and set aside solely for this purpose. Thus, they act as master reference cells with their I_{REF}'S used as reference levels for the reading and programming of all other EEprom cells on the same chip. By using the same device as the EEprom cells to act as reference cells, excellent tracking with respect to temperature, voltage and process variations is achieved. Furthermore, the charge retention problem, important in multi-state implementation, is alleviated.

Referring to FIG. **17**A, one such master reference cell **1400** is shown with its program and read paths. The reference cells erase and program module **1410** serves to program or re-program each such reference cell **1400**. The module **1410** includes program and erase circuits **1411** with a programming path **1413** connected to the drain of the master reference call **1400**. The circuits **1411** are initiated by addresses decoded from the internal bus **1111** by a program decoder **1415** and an erase decoder **1417** respectively. Accordingly, programming voltages or erasing voltages are selectively supplied each reference cell such as cell **1400**. In this way, the reference level in each reference cell may be independently set cr reprogrammed. Typically, the threshold level of each reference cell will be factory-programmed to the optimum level appropriate to each batch of chips produced. This. could be done by comparison with an external standard reference level. By software control, a user also has the option to reset the reference threshold levels.

Once the reference threshold voltage V_{T1} or reference drain-source current I_{REF} is programmed into each reference cell **1400**, it then serves as a reference for the reading of an addressed memory cell such as cell **1420**. The reference cell **1400** is connected to a first leg **1403** of a current sensing amplifier **1410** via a clocked switch **1413**. A second leg **1415** of the amplifier is essentially connected to the addressed memory cell **1420** whose programmed conduction state is to be determined. When cell **1420** is to be read, a control signal READ will enable a switch **1421** so that the cell's drain is connected to the second leg **1415**. The sense amplifier **1410** supplies voltage via V_{CC} to the drains of both the master reference cell **1400** and the addressed cell **1420**. In the preferred embodiment, the amplifier has a current mirror configuration such that any differential in currents through the two legs **1403** and **1415** results in the voltage in the second leg **1415** being pulled up towards V_{CC} or down towards V_S Thus, the node at the second leg **1415** is respectively HIGH (or LOW) when the source-drain current I_{DS} for the addressed cell **1420** is less (or more) than I_{REF} through the master reference cell **1400**. At the appropriate time controlled by a clocked switch **1423**, the sensed result at the second leg **1415** may be held by a latch **1425** and made available at an output line **1427**. When I_{DS} is less than I_{REF}, a HIGH appears at the output line **1427** and the addressed cell **1420** is regarded as in the same conduction state as the master reference cell **1400**.

In the preferred embodiment, a voltage clamp and fast pull-up circuit **1430** is also inserted between the second leg **1415** and the drain **1431** of the addressed cell **1420**. The circuit **1430** serves to keep the drain voltage VD at a maximum of 1.5 V–2.0 V when it is charging up in the case of lower I_{DS}. It also prevents V_D from pulling too low in the case of higher I_{DS}.

In general, if each memory cell is to store K states, then at least K−1, or preferably K reference levels need be provided. In one embodiment, the addressed cell is compared to the K reference cells using k sense amplifiers in parallel. This is preferable for the 2-state case because of speed, but may spread the available current too thin for proper sensing in the multi-state case. Thus, for multi-state case, it is preferable to compare the addressed cell with the K reference cells one at a time in sequence.

FIG. **17**B illustrates more explicitly the multi-state reading configuration. The K reference cells such as **1431**, **1433**, **1435** are connected to the sense amplifier **1440** via the amplifier's first leg **1441**. The connection is time-multiplexed by clocked switches such as **1451**, **1453**, **1455** respectively. The second leg **1457** of the sense amplifier is connected to the addressed cell as in FIG. **17**A. The sensed signal at the second leg **1457** is time-selectively latched by clocked switches such as **1461**, **1463**, **1465** onto such latches **1471**, **1473**, **1475**.

FIGS. **17**C(**1**)–**17**C(**8**) illustrate the timing for multistate read. When the signal READ goes HIGH, a switch **1421** is enabled and the addressed memory cell is connected to the second leg **1457** of the sense amplifier **1440** (FIG. **17**C(**1**)). The clocks timing is given in FIGS. **17**C(**2**)–**17**C(**4**). Thus, at each clock signal, the sense amplifier sequentially compares the addressed cell with each of the reference cells and latches each results. The latched outputs of the sense amplifier are given in FIGS. **17**C(**5**)–**17**C(**7**). After all the K output states of the sense amplifier **1440** are latched, they are encoded by a K–L decoder **1480** ($2^L \geqq K$) (FIG. **17**C(**8**)) into L binary bits.

Thus, the multiple threshold levels are provided by a set of memory cells which serves as master reference cells. The master reference cells are independently and externally erasable and programmable, either by the device manufacturer or the user. This feature provides maximum flexibility, allowing the breakpoint thresholds to be individually set within the threshold window of the device at any time. By virtue of being the same device as that of the memory cells, the reference cells closely track the same variations due to manufacturing processes, operating conditions and charge retention problems. The independent programmability of each threshold level at will allows optimization and fine-tuning of the partitioning of the threshold window to make multi-state memory viable. Furthermore, it allows post-manufacture configuration for either 2-state or multi-state memory from the same device, depending on user need or device characteristics at the time.

Another important feature of the present invention serves to overcome the problems of endurance-related stress. As explained previously, the erase, program and read characteristics of each memory cell depends on the cumulated stress endured over the number of program/erase cycles the cell has been through. In general, the memory cells are subjected to many more program/erase cycles than the master reference cells. The initially optimized reference levels will eventually become misaligned to cause reading errors. The present underlying inventive concept is to have the reference levels also reflect the same cycling suffered by the memory cells. This is achieved by the implementation of local reference cells in addition to the master reference cells. The local reference cells are subjected to the same program/erase cycling as the memory cells. Every time after an erase operation, the reference levels in the master reference cells are re-copied into the corresponding set of local reference cells. Memory cells are then read with respect to the reference levels of the closely tracking local reference cells.

In this way, the deviation in cell characteristics after each program/erase cycle is automatically compensated for. The proper partitioning of the transforming threshold window is therefore maintained so that the memory states can be read correctly even after many cycles.

FIG. **18** illustrates the local cells referencing implementation for Flash EEprom. In the Flash EEprom array **1060** (FIG. **12**), each group of memory cells which is collectively erased or programmed is called a sector. The term "Flash sector" is analogous to the term "sector" used in magnetic disk storage devices and they are used interchangeably here. The EEprom array is grouped into Flash sectors such as **1501**, **1503** and **1505**. While all memory cells in a Flash sector suffer the same cycling, different Flash sectors may undergo different cycling. In order to track each Flash sector properly, a set of memory cells in each Flash sector is set aside for use as local reference cells. For example, after the Flash sector **1503** has been erased, the reference levels in the master reference cells **1507** are re-programmed into the local reference cells associated with the Flash sector **1503**. Until the next erase cycle, the read circuits **1513** will continue to read the memory cells within the Flash sector **1503** with respect to the re-programmed reference levels.

FIGS. **19(1)–19(7)** illustrates the algorithm to reprogram a sector's reference cells. In particular, FIGS. **19(1)–19(3)** relate to erasing the sector's local reference cells to their "erased states". Thus in FIG. **19(1)**, a pulse of erasing voltage is applied to all the sector's memory cells including the local reference cells. In FIG. **19(2)**, all the local reference cells are then read with respect to the master references cells to verify if they have all been erased to the "erased state". As long as one cell is found to be otherwise, another pulse of erasing voltage will be applied to all the cells. This process is repeated until all the local reference cells in the sector are verified to be in the "erased" state (FIG. **19(3)**).

FIGS. **19(4)–19(7)** relate to programming the local reference cells in the sector. After all the local reference cells in the sector have been verified to be in the "erased" state, a pulse of programming voltage is applied in FIG. **19(4)** only to all the local reference cells. This is followed in FIG. **19(5)** by reading the local reference cells with respect to the master reference cells to verify if every one of the local reference cells is programmed to the same state as the corresponding master reference cell. For those local reference cells not so verified, another pulse of programming voltage is selectively applied to them alone (FIG. **19(6)**). This process is repeated until all the local reference cells are correctly verified (FIG. **19(7)**) to be programmed to the various breakpoint threshold levels in the threshold window.

Once the local reference cells in the sector have been re-programmed, they are used directly or indirectly to erase verify, program verify or read the sector's addressed memory cells.

FIG. **20A** illustrates one embodiment in which the local reference cells are used directly to read or program/erase verify the sector's memory cells. Thus, during those operations, a parallel pair of switches **1525** is enabled by a READ signal and the sense amplifier **1440** will read the sector's addressed memory cells **1523** with respect to each of the sector's local reference cells **1525**. During program/erase verify of the local reference cells (as illustrated in FIG. **19**), another parallel pair of switches **1527** enables reading of the local reference cells **1525** relative to the master reference cells **1529**.

FIG. **20B** illustrates the algorithm for using the local reference cells directly to read or program/erase verify the sector's addressed memory cells.

FIG. **21A** illustrates an alternative embodiment in which the local reference cells are used indirectly to read the addressed memory cells. First the master reference cells are erased and programmed each to one of the desired multiple breakpoint thresholds within the threshold window. Using these master reference thresholds the local reference cells within an erased sector of cells are each programmed to one of the same desired multiple breakpoint thresholds. Next the addressed cells in the sector are programmed (written) with the desired data. The reading sequence for the addressed cells in the sector then involves the steps illustrated in FIG. **21A**.

First each of the local reference cells **1525** is read relative to the corresponding master reference cell **1531**. This is effected by an enabling READ I signal to a switch **1533** connecting the local reference cells **1525** to the second leg **1457** of the sense amplifier **1440** with the master reference **1531** connected to the first leg **1441** of the sense amplifier. Auxiliary current source circuits associated with each master reference cell are now used to optimally bias the current through the first leg **1441** of the sense amplifier to match the current in the second leg **1457**. After the bias adjustment operation is completed for all breakpoint threshold levels the addressed cells in the sector are read relative to the bias-adjusted master reference cells. This is effected by disabling READ I to **1533** and enabling READ signal to switch **1535**. The advantage of this approach is that any variations in V_{CC}, temperature, cycling fatigue or other effects which may, over time, cause threshold deviations between the master reference cells and the addressed cells is eliminated prior to reading, since the local reference cells (which track threshold deviations of the addressed cells) are used to effectively readjust the breakpoint thresholds of the master reference cells. For example, this scheme permits programming of the addressed cells when the master reference cells are powered with V_{CC}=5.5 V and subsequently reading the addressed cells with the master reference cells powered at V_{CC}=4.5 V. The difference of 1 volt in V_{CC}, which would normally cause a change in the value of the breakpoint thresholds, is neutralized by using the local reference cells to bias adjust the master reference cells to counteract this change at the time of reading.

FIGS. **21B** and **21C** show in more detail one embodiment of the current biasing circuits such as **1541**, **1543**, **1545** for the master reference cells **1551**, **1553**, **1555**. Each biasing circuit acts as a current shunt for the current in the master reference cell. For example, the circuit **1541** is tapped to the drain of the master reference cell **1551** through the line **1561**. It modifies the current in line **1562** to the sense amplifier (first leg) either by sourcing current from V_{CC} or draining current to V_{SS}. In the former case, the current in the line **1562** is reduced, and otherwise for the latter case. As biasing is being established for the master reference **1551**, any inequality in the currents in the two legs of the sense amplifier can be communicated to outside the chip. This is detected by the controller (see FIG. **13**) which in turn programs the biasing circuit **1541** via the internal address bus **1111** to subtract or add current in the line **1562** in order to equalize that of the local reference.

FIG. **21C** illustrates an embodiment of the biasing circuit such as the circuit **1541**. A bank of parallel transistors such as **1571**, **1573**, **1575** are all connected with their drains to V_{CC}, and their sources via switches such as **1581**, **1583**, **1585** to the line **1561**. By selectively enabling the switches, different number of transistors may be used to subtract various amount of current from line **1562**. Similarly, another bank of parallel transistors such as **1591**, **1593**, **1595** are all

connected with their sources to V_{SS}, and their drains via switches such as **1601**, **1603**, **1605** to the line **1561**. By selectively enabling the switches, a different number of transistors may be used to add a various amount of current to line **1562**. A decoder **1609** is used to decode address from the internal address bus **1111** to selectively enable the switches. The enabling signals are stored in latches **1611**, **1613**. In this way every time a sector is read, the master reference cells are re-biased relative to the local reference cells, and used for reading the memory cells in the sector.

FIGS. **21D(1)–21D(4)** illustrate the read algorithm for the alternative embodiment. The sector must previously have had its local reference cells programmed and verified relative to the master reference cells (FIG. **21D(1)**). Accordingly, each of the master reference cells is then read relative to the local reference cells (FIG. **21D(2)**). The master reference cells are biased to equalize the current to that of the corresponding local reference cells (FIG. **21D(3)**). Subsequently, the memory cells in the sector are read relative to the biased master reference cells(FIG. **21D(4)**).

The read circuits and operation described are also employed in the programming and erasing of the memory cells, particularly in the verifying part of the operation. As described previously, programming is performed in small steps, with reading of the state programmed in between to verify if the desired state has been reached. As soon as the programmed state is verified correctly, programming stops. Similarly, erasing is performed in small steps, with reading of the state of erase in between to verify if the "erased" state has been reach. Once the "erased" state is verified correctly, erasing stops.

As described previously, only K−1 breakpoint threshold levels are required to partition the threshold window into K regions, thereby allowing the memory cell to store K states. According to one aspect of the present invention, however, in the multi-state case where the threshold window is more finely partitioned, it is preferable to use K threshold levels for K state. The extra threshold level is used to distinguish the "erased" state from the state with the lowest threshold level. This prevents over-erasing and thus over-stressing the cell since erasing will stop once the "erased" state is reached. The selective inhibition of individual cells for erase does not apply to the Flash EEprom case where at least a sector must be erased each time. It is suitable for those EEprom arrays where the memory cells can be individually addressed for erase.

According to another feature of the invention, after a memory cell has been erased to the "erased" state, it is programmed slightly to bring the cell to the state with the lowest threshold level (ground state) adjacent the "erased" state. This has two advantages. First, the threshold levels of the ground state of all the memory cells, being confined between the same two breakpoint threshold levels, are well-defined and not widely scattered. This provide an uniform starting point for subsequent programming of the cells. Secondly, all cells get some programming, thereby preventing those cells which tend to have the ground state stored in them, for example, from losing track with the rest with regard to program/erase cycling and endurance history.

On Chip Program Verify

As mentioned before, programming of an EEprom cell to a desired state is preferably performed in small steps starting from the "erase" state. After each programming step, the cell under programming is read to verify if the desired state has been reached. If it has not, further programming and verifying will be repeated until it is so verified.

Referring to the system diagram illustrated in FIG. **13**, the EEprom chip **1130** is under the control of the controller **1140**. They are linked serially by the serial in line **1251** and serial out line **1253**. In prior art EEprom devices, after each programming step, the state attained in the cell under programming is read and sent back to the controller **1140** or the CPU **1160** for verification with the desired state. This scheme places a heavy penalty on speed especially in view of the serial link.

In the present invention, the program verification is optimized by programming a chunk (typically several bytes) of cells in parallel followed by verifying in parallel and on chip. The parallel programming is implemented by a selective programming circuit which disables programming of those cells in the chunk whose states have already been verified correctly. This feature is essential in a multi-state implementation, because some cells will reach their desired state earlier than others, and will continue past the desired state if not stopped. After the whole chunk of cells have been verified correctly, logic on chip communicates this fact to the controller, whereby programming of the next chunk of cells may commence. In this way, in between each programming step data does not need to be shuttled between the EEprom chip and the controller, and program verification speed is greatly enhanced.

FIG. **22** illustrates the program and verify paths for a chunk of n cells in parallel. The same numerals are used for corresponding modules in the system diagram of FIG. **13**. The EEprom array **1060** is addressed by N cells at a time. For example, N may be 64 cells wide. In a 512 bytes Flash sector, consisting of 4 rows of 1024 cells, there will be 64 chunks of 64 cells. The source multiplexer **1107** selectively connects the N sources of one addressed chunk of cells to the source voltage V_S in line **1103**. Similarly, the drain multiplexer **1109** selectively makes the N drains of the chunk accessible through an N-channel data path **1105**. The data path **1105** is accessed by the program circuit with inhibit **1210** during programming and by read circuits **1220** during reading, program verifying or erase verifying.

Referring again to the system diagram in FIG. **13**, programming is under the control of the controller **1140**. The data to be programmed into the sector is sent chunk by chunk. The controller first sends a first chunk of N*L serial data bits together with addresses, control and timing information to the EEprom chip **1130**. L is the number of binary bits encoded per memory cell. For example, L=1 for a 2-state cell, and L=2 for a 4-state cell. Thus if N=64 and L=2, the chunk of data bits will be 128 bits wide. The N*L data bits are stored in latches and shift registers **1190** where the serial bits are converted to N*L parallel bits. These data will be required for program verify in conjunction with the read circuits **1220**, bit decoder **1230**, compare circuit **1200** and the program circuit with inhibit **1210**.

The program algorithm for a chunk of N cells is best described by referring to both the system diagram of FIG. **13** and FIGS. **23(1)–23(7)** which illustrate the algorithm itself. As mentioned in an earlier section, prior to programming the sector, the whole sector must be erased and all cells in it verified to be in the "erased" state (FIG. **23(1)**). This is followed in FIG. **23(2)** by programming the sector local reference cells (as shown in FIGS. **19(1)–(3)**). In FIG. **23(3)**, the N*L bits of parallel data is latched in latches **1190**. In FIG. **23(4)**, the read circuits **1220** access the N-channel data path **1105** to read the states in the N chunk of cells. The read algorithm has already been described in conjunction with FIG. **20B** or FIG. **21D**. The N-cell reads generates N*K (K=number of states per cell) output states. These are decoded by bit decoder **1230** into N*L binary bits. In FIG. **23(5)**, the N*L read bits are compared bit by bit with the

N*L program data bits from latches **1190** by compare circuit **1200**. In FIG. **23(6)**, if any read bit fails to compare with the program data bit, a further programming voltage pulse from the program circuit **1210** is applied simultaneously to the chunk of cells. However, an inhibit circuit within the program circuit **1210** selectively blocks programming to those cells whose bits are correctly verified with the programmed data bits. Thus, only the unverified cells are programmed each time. Programming and verification are repeated until all the cells are correctly verified in FIG. **23(7)**.

FIG. **24** shows one embodiment of the compare circuit **1200** of FIG. **13** in more detail. The circuit **1200** comprises N cell compare modules such as **1701**, **1703**, one for each of the N cells in the chunk. In each cell compare module such as the module **1701**, the L read bits (L=number of binary bits encoded for each cell) are compared bit by bit with the corresponding program data bits. This is performed by L XOR gates such as **1711**, **1713**, **1715**. The output of these XOR gates pass through an NOR gate **1717** such that a "1" appears at the output of NOR gate **1717** whenever all the L bits are verified, and a "0" appears when otherwise. When the control signal VERIFY is true, this result is latched to a latch **1721** such that the same result at the output of NOR gate **1717** is available at the cell compare module's output **1725**. The compare circuit **1200** performs the comparisons of L bits in parallel. The N compare module's outputs such as **1725**, **1727** are available at an N-channel output line **1731** to be fed to the program circuit with inhibit **1210** of FIG. **13**.

At the same time, the N outputs such as **1725**, **1727** are passed through an AND gate **1733** so that its single output **1735** results in a "1" when all N cells are verified and a "0" when otherwise. Referring also to FIG. **13**, the single output **1735** is used to signal the controller **1140** that all N cells in the chunk of data have been correctly verified. The signal in output **1735** is sent through the serial out line **1253** via AND gate **1240** during a VERIFY operation.

At power-up or at the end of program/verify of a chunk of data, all cell compare module's outputs such as **1725**, **1727** are reset to the "not-verified" state of "0". This is achieved by pulling the node **1726** to V_{SS} (0 V) by means of the RESET signal in line **1727** to a transistor **1729**.

FIG. **25** shows one embodiment of the program circuit with inhibit **1210** of FIG. **13** in more detail. The program circuit **1210** comprises N program with inhibit modules such as **1801**, **1803**. As illustrated in the tables of FIGS. **26** and **27**, in order to program the N cells, a voltage V_{PD} must be applied to each of the N cells' drain and a voltage V_{PG} applied to the control gates. Each program module such as **1801** serves to selectively pass V_{PD} on a line **1805** to one of the drains through the one of the N-channel data path **1105**. Since V_{PD} is typically about 8 V to 9 V which is higher than V_{CC}, the latter cannot be used to turn on the transistor switch **1807**. Rather the higher voltage V_{CG} (about 12 V) is used to enable switch **1807**. V_{CG} in line **1801** is itself enabled by an AND gate when both the program control signal PGM in line **1813** is true and the signal in line **1731** is a "0". Since the signal in line **1731** is from the output of the cell compare module **1701** shown in FIG. **24**, it follows that V_{PD} will be selectively passed onto those cells which are not yet verified. In this way, every time a programming pulse is applied, it is only applied to those cells which have not yet reached their intended states. This selective programming feature is especially necessary in implementing parallel programming and on chip verification in the multi-state case.

Variable Control of Voltage to the Control Gate

The system diagram of FIG. **13** in conjunction with FIGS. **26** and **27** illustrate how various voltages are applied to the EEprom array **1060** to perform the basic functions of the EEprom. Prior art EEprom devices only allow the voltage supplied to the control gate V_{CG} to assume one of two voltages, namely V_{CC} or the higher programming voltage of about 12 V.

In another aspect of the present invention, the voltage supplied to the control gate V_{CG} is allowed to be independently and continuously variable over a wide range of voltages. This is provided by V_{PG} from the controller **1140**. In particular V_{CG} in a line **1083** is fed from V_{PG} which is in turn supplied by the controller from a line **1901**. FIG. **27** shows V_{PG} to assume various voltages under different functions of the EEprom.

The variability of V_{CG} is particularly advantageous in program and erase margining schemes. In program margining, the read during program verify is done with V_{CG} at a slightly higher voltage than the standard V_{CC}. This helps to place the programmed threshold well into the state by programming past the breakpoint threshold level with a slight margin. In erase verify, the cell is verified with a somewhat reduced V_{CG} to put the cell well into the "erased" state. Furthermore, margining can be used to offset the charge retention problem described earlier (FIG. **16B**).

As mentioned before, prior art EEproms typically employ V_{CC} to feed V_{CG} during program or erase verify. In order to do margining, V_{CC}, itself needs to be ramped up or reduced. This practice produces inaccurate results in the reading circuits since they are also driven by V_{CC}.

In the present invention, the variability of V_{CG} independent of voltages supplied to the reading circuit produce more accurate and reliable results.

Furthermore, the wide range of V_{CG} is useful during testing and diagnostic of the EEprom. It allows the full range of the programmed cell's threshold to be measured easily by continuing to increase V_{CG} (up to the maximum limited by the device's junction breakdown).

While the embodiments of the various aspects of the present invention that have been described are the preferred implementation, those skilled in the art will understand that variations thereof may also be possible. Therefore, the invention is entitled to protection within the full scope of the appended claims

We claim:

1. A method of operating an EEprom system having memory cells that individually include an electrically floating gate carrying a charge level that is alterable in response to appropriate voltage conditions being applied to the cell in order to set a variable threshold level thereof into a range that is determinable by reading the cell, said method comprising:

applying said appropriate voltage conditions in parallel to a plurality of said memory cells, thereby to alter the charge levels on the floating gates of said plurality of memory cells,

determining the threshold level ranges in which individual ones of said plurality of memory cells lie, and

terminating said application of appropriate voltage conditions to individual ones of said plurality of memory cells upon their being determined to have reached desired threshold level ranges while continuing to apply said appropriate voltage conditions to others of said plurality of cells until all of the plurality of cells are determined to have reached their desired threshold level ranges.

2. The method of claim **1**, wherein there are exactly two threshold level ranges.

3. The method of claim **1**, wherein there are more than two threshold level ranges.

4. The method of claim 1, wherein the threshold level ranges are separated by exactly one breakpoint threshold level, thereby to provide exactly two non-overlapping threshold level ranges.

5. The method of claim 1, wherein the threshold level ranges are separated by more than one breakpoint threshold level, thereby to provide more than two non-overlapping threshold level ranges.

6. The method of claim 1, wherein said desired threshold level ranges include an erased threshold level range.

7. The method of claim 1, wherein the array of memory cells are grouped into blocks of cells wherein the threshold levels of cells within a selected one of the blocks are changed together to a single given threshold level range prior to applying said appropriate voltage conditions in parallel to the plurality of cells within said one block.

8. The method of claim 7, wherein individual ones of said blocks include a specific number of memory cells and said plurality of memory cells to which said appropriate voltage conditions are applied in parallel are less than said specific number, and additionally comprising repeating for another plurality of cells within said one block said applying, determining and terminating operations.

9. The method of claim 7, wherein individual ones of the blocks of cells contain a number of spare cells, and further wherein the spare cells within a particular block are substituted in place of any defective cells within said plurality of cells of said particular block.

10. The method of any one of claims 1–9, carried out on a single integrated circuit chip.

11. The method of claim 1, wherein the array of memory cells are grouped into blocks of cells wherein the threshold levels of cells within individual ones of the blocks are changed together to a single given threshold level range prior to applying said appropriate voltage conditions in parallel to the plurality of cells within one of the blocks, the method further comprising simultaneously changing the threshold levels of cells within a selected two or more blocks to said given level range.

12. The method of claim 1 wherein the desired ones of said threshold level ranges reached by applying appropriate voltage conditions to the plurality of memory cells correspond to a chunk of input data being programmed into the memory system.

13. The method of claim 12, wherein the plurality of cells are determined to have reached the desired threshold level ranges by comparing the threshold levels of the plurality of cells with the chunk of input data.

14. The method of claim 13, wherein the chunk of input data is stored in a cache memory prior to being programmed into memory cells within the EEprom.

15. The method of claim 5, wherein the appropriate voltage conditions are applied to said plurality of memory cells in successive applications of said voltage pulses that individually shift the threshold level of the cells to which the voltage pulses are applied less than one half of a difference between adjacent ones of the breakpoint levels.

16. The method of either of claims 3 or 5, wherein terminating the application of appropriate voltage conditions to individual ones of the plurality of memory cells occurs upon their being determined to have been programmed to within the desired threshold levels by a margin.

17. The method of any one of claims 1, 2 or 4, wherein individual ones of the plurality of memory cells are determined to have reached their desired threshold level ranges by comparison with at least one reference level stored in at least one of the memory cells.

18. The method of either of claims 3 or 5, wherein individual ones of the plurality of memory cells are determined to have reached their desired threshold level ranges by comparison with two or more reference levels stored in two or more of the memory cells.

19. An electrically erasable and programmable read only memory system, comprising:

an array of electrically alterable memory cells that individually include a field effect transistor having a floating gate and a threshold level that is variable in accordance with an amount of charge carried by the floating gate, said array being divided into blocks of cells that are resettable together, cells within said blocks being addressable for application of programming voltage conditions to individually program them into one of more than two distinct threshold level ranges corresponding to more than one bit of input data per cell,

a reset circuit that simultaneously applies reset voltage conditions to the cells within individual blocks to drive the effective threshold levels of such cells to a reset state,

a programming circuit that applies the programming voltage conditions to a plurality of addressed cells within a reset block to drive the effective threshold voltage of the addressed cells toward one of the more than two programmable threshold level ranges,

a reading circuit that monitors in parallel the threshold level ranges of the plurality of addressed cells, and

a control circuit that individually terminates application of the programming voltage conditions to any one of the plurality of addressed cells when the reading circuit verifies that said any one cell has reached the programmable threshold level range that corresponds to the input data being stored therein, while enabling further application of the programming voltage conditions to others of the plurality of addressed cells that have not yet been so verified, until all of the plurality of addressed cells are verified.

20. The memory system according to claim 18, wherein the plurality of addressed cells are less than a number of cells within the individual blocks.

21. The memory system according to claim 19, wherein the control circuit includes a plurality of latches and means for setting individual ones of the latches in response to corresponding ones of said plurality of addressed cells being verified.

22. The memory system according to claim 19, wherein said more than two distinct threshold level ranges are non-overlapping and separated from each other by two or more breakpoint threshold levels.

23. The memory system according to claim 22, wherein the reading circuit includes means for ascertaining the individual threshold level ranges of the plurality of memory cells after the cells have been programmed into the individual threshold level ranges beyond one of their breakpoints by a margin.

24. The memory system according to claim 19, wherein the programming circuit causes the plurality of addressed cells to be programmed with successive applications of said programming voltage conditions, and the reading circuit operates to monitor the threshold level ranges of the plurality of addressed cells in between applications of said programming voltage conditions.

25. The memory system according to claim 24, wherein the programming circuit further shifts the threshold levels of

the individual addressed cells by less than one half of a difference between at least two breakpoint threshold levels defining one of the threshold level ranges.

26. The memory system according to claim **24**, wherein the programming circuit further operates with programming voltage conditions that requires a plurality of said successive applications of programming voltage conditions in order to change individual ones of the plurality of addressed cells from one of the threshold level ranges to another adjacent threshold level range.

27. The memory system according to claim **19**, wherein the control circuit includes a comparator receiving the monitored threshold level range of the plurality of addressed cells and the input data being programmed into the plurality of addressed cells for verifying when the individual ones of the plurality of cells reach the programmable threshold level that corresponds to the input data being stored therein.

28. The memory system according to claim **19**, wherein at least one reference cell is included in individual ones of the blocks of cells, and which additionally comprises means for programming said at least one reference cell to a reference level, and wherein said reading circuit includes means for reading the reference level of the reference cell of the block wherein the plurality of addressed cells exists to verify that any one cell has reached the desired threshold level range.

29. The memory system according to claim **19**, wherein the reset circuit includes means operable after application of the reset voltage conditions to an addressed at least one block for adjusting to the reset state any cells of said at least one block that were overerased by the reset voltage condition application.

30. The memory system according to claim **19**, wherein the reset circuit includes means for selecting one or more of the blocks for erase, and means responsive to the selection means for simultaneously applying the reset voltage condition to the memory cells within all of the selected blocks.

31. The memory system according to claim **30**, wherein the block selecting means includes a register associated with individual ones of the blocks for containing an indication whether the associated block is to be erased.

32. A method of storing multiple bits of binary data in a chunk of non-volatile memory cells which individually have more than two programmable states, comprising:

applying electrical programming parameters in parallel to cells within said chunk,

monitoring the states of individual cells within said chunk, and

terminating application of programming parameters to individual cells within said chunk when they are monitored to have reached desired ones of said more than two programmable states corresponding to the multiple bits of data being stored, while continuing to apply said programming parameters to others of the cells within said chunk, until all of the cells within said chunk are determined to have reached their programmable states corresponding to the multiple bits of data being stored.

33. The method of claim **32**, wherein, prior to applying electrical programming parameters to cells within said chunk, at least the cells within said chunk are all reset to a common state different than any of said more than two programmable states.

34. The method of claim **32**, wherein, prior to applying electrical programming parameters to the cells wherein said chunk, at least the cells within said chunk are all reset to one of the more than two programmable states.

35. The method of claim **34**, wherein resetting at least the cells within said chunk includes initially driving at least all of the cells within said chunk to a common state different than any of said more than two programmable states, and then programming all of at least the cells within said chunk from the common state into one of the more than two programmable states by the following:

applying electrical programming parameters in parallel to at least the cells within said chunk,

monitoring the states in which at least the cells within said chunk are individually programmed, and

terminating application of programming parameters to individual ones of at least the cells within said chunk when they are monitored to have reached said one of the more than two programmable states while continuing to apply said programming parameters to others of the cells within said chunk until all of the cells within said chunk are determined to have reached the said one of the more than two programmable states.

36. An electrically erasable and programmable non-volatile memory system, comprising:

an integrated circuit array of electrically alterable memory cells that are individually programmable into more than two states, thereby individually storing more than one bit of binary data,

a programming circuit that applies appropriate programming parameters in parallel to an addressed plurality of cells,

a reading circuit that verifies in parallel the state into which the addressed plurality of cells are programmed,

means for inhibiting further programming of correctly verified cells among the plurality of addressed cells, and

means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly.

37. A method of operating an EEprom system having memory cells that individually include an electrically floating gate carrying a charge level that is alterable in response to appropriate voltage conditions being applied to the cell in order to set a variable threshold thereof to a desired level that is determinable by reading the cell, said method comprising:

applying said appropriate voltage conditions in parallel to a plurality of said memory cells, thereby to alter the charge levels on the floating gates of said plurality of memory cells to drive their threshold levels to desired levels,

individually monitoring the threshold levels of said plurality of memory cells to set a binary element associated with each such cell, when reaching its desired threshold level, in order to prevent further application of appropriate voltage conditions to said plurality of memory cells from altering the charge level of the associated memory cell, and

continuing the voltage applying and monitoring steps until all of said plurality of cells have reached their desired levels without allowing any individual binary element to be reset as a result of any monitoring its associated memory cell after the binary element is set.

38. The method of claim **37**, wherein there are exactly two threshold levels.

39. The method of claim **37**, wherein there are more than two threshold levels.

* * * * *

EXHIBIT K

United States Patent [19]

Yuan et al.

[11] Patent Number: 5,070,032

[45] Date of Patent: Dec. 3, 1991

[54] METHOD OF MAKING DENSE FLASH EEPROM SEMICONDUCTOR MEMORY STRUCTURES

[75] Inventors: **Jack H. Yuan**, Cupertino; **Eliyahou Harari**, Los Gatos, both of Calif.

[73] Assignee: **SunDisk Corporation**, Santa Clara, Calif.

[21] Appl. No.: **323,779**

[22] Filed: **Mar. 15, 1989**

[51] **Int. Cl.**[5] **H01L 21/265**

[52] **U.S. Cl.** **437/43**; 437/49; 437/52; 437/233

[58] **Field of Search** 437/43, 52, 195, 968, 437/983, 193; 357/23.5

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,239,559	12/1980	Ito	437/968
4,804,637	2/1989	Smayling et al.	437/43
4,814,286	3/1989	Tam	437/43
4,852,062	7/1989	Baker et al.	365/185
4,853,895	8/1989	Mitchell et al.	437/43

FOREIGN PATENT DOCUMENTS

349774	1/1990	European Pat. Off. .
0003976	1/1984	Japan .

OTHER PUBLICATIONS

Mizutani and Makita, "A New EPROM Cell with a Side-wall Floating Gate for High-Density and High-Performance Device", *IDEM 85*, pp. 635-639, 1985.

Primary Examiner—Brian E. Hearn

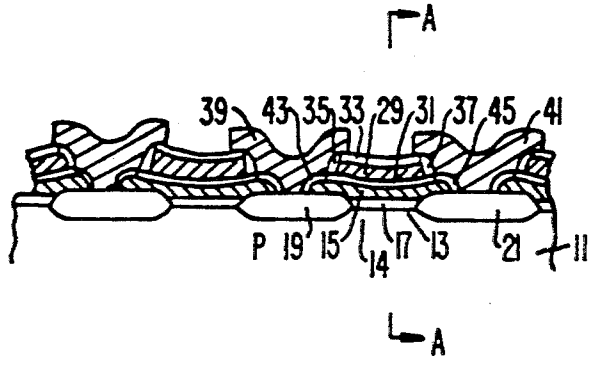
Assistant Examiner—Chandra Chaudhari

Attorney, Agent, or Firm—Majestic, Parsons, Siebert & Hsue

[57] **ABSTRACT**

An improved electrically erasable and programmable read only memory (EEprom) structure and processes of making it which results in a denser integrated circuit, improved operation and extended lifetime. In order to eliminate certain ill effects resulting from tolerances which must be allowed for registration of masks used in successive steps in forming the semiconductor structures, spacers are formed with reference to the position of existing elements in order to form floating gates and define small areas of these gates where, in a controlled fashion, a tunnel erase dielectric is formed. Alternatively, a polysilicon strip conductor is separated into separate control gates by a series of etching steps that includes an anisotropic etch of boundary oxide layers to define the area of the control gates that are coupled to the erase gate through an erase dielectric. In either case, the polysilicon layer strip can alternatively be separated by growing oxide thereon until it is completely consumed. A technique for forming a pure oxide dielectric layer of uniform thickness includes depositing a thin layer of an undoped polysilicon material and then oxidizing its surface until substantially the entire undoped polysilicon layer is consumed and made part of the resulting oxide layer. Overlapping doped regions are provided in the substrate by an ion implantation mask that adds spacers to the mask aperture to change its size between implants.

30 Claims, 6 Drawing Sheets



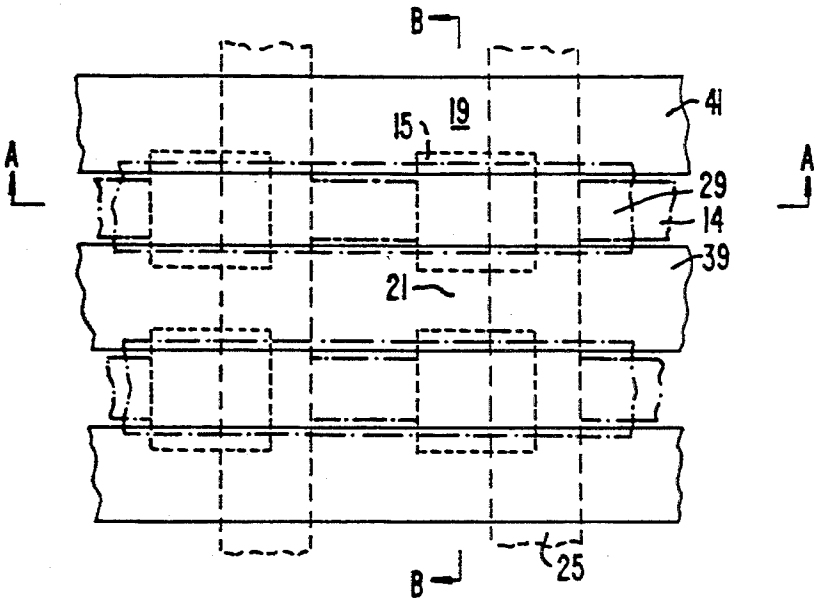


FIG._1.

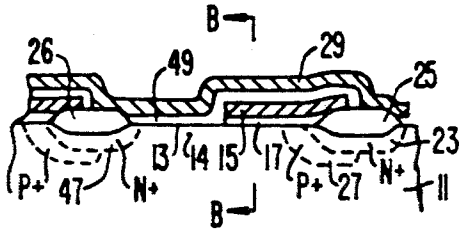


FIG._2A.

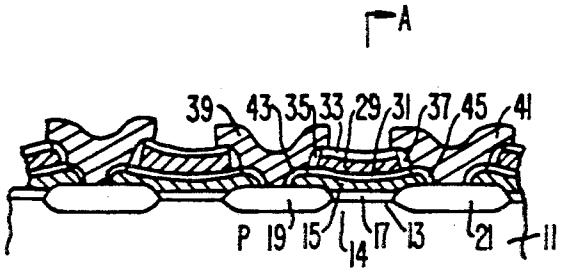


FIG._2B.

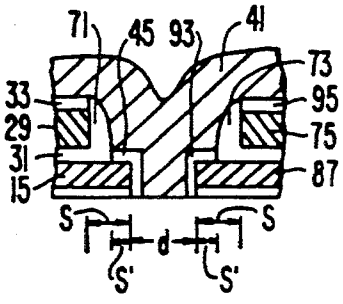


FIG._13.

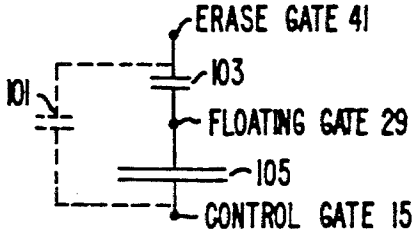


FIG._14.

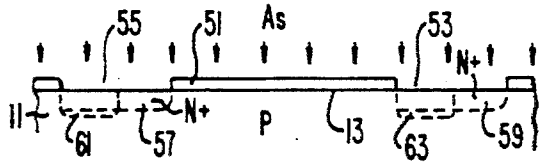


FIG._4A.

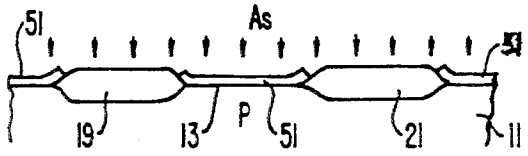


FIG._4B.

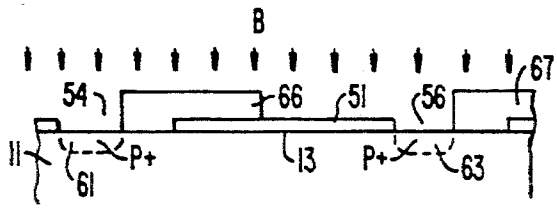


FIG._3A.

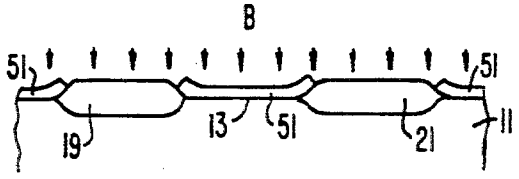


FIG._3B.

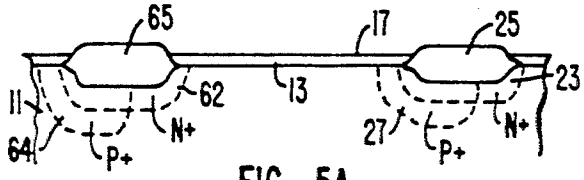


FIG._5A.

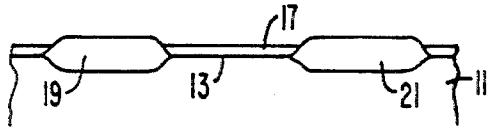


FIG._5B.

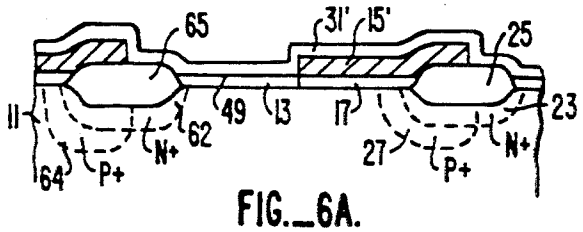


FIG._6A.

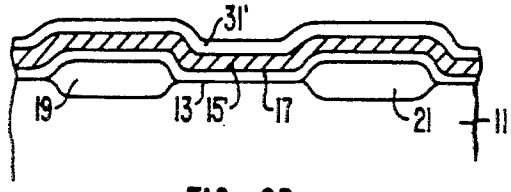


FIG._6B.

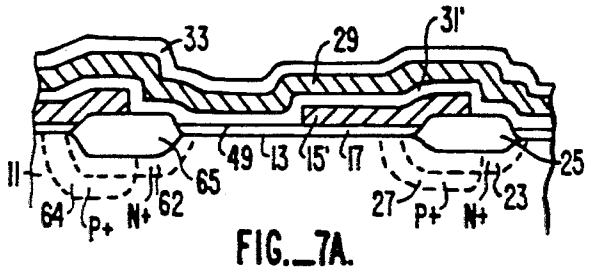


FIG._7A.

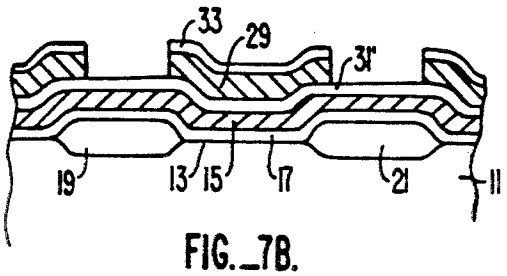


FIG._7B.

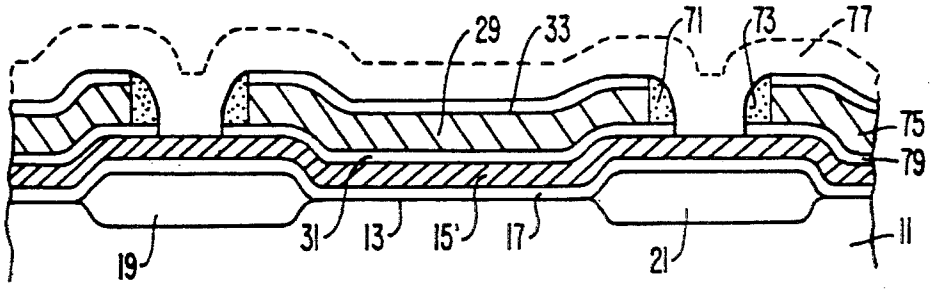


FIG._8.

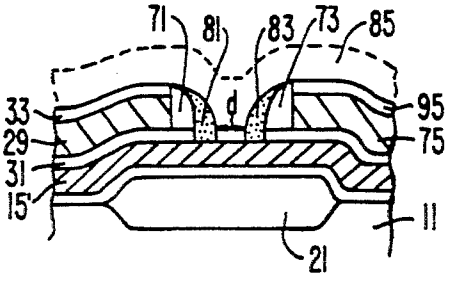


FIG._9.

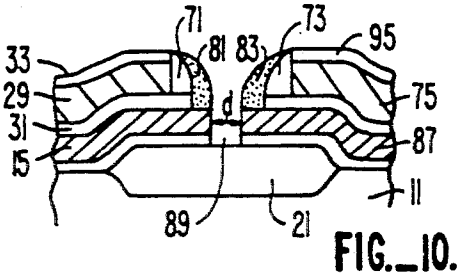


FIG._10.

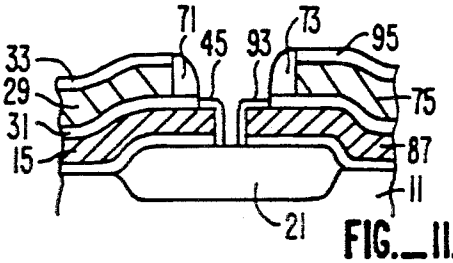


FIG._11.

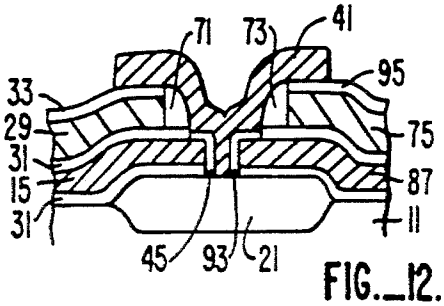


FIG._12.

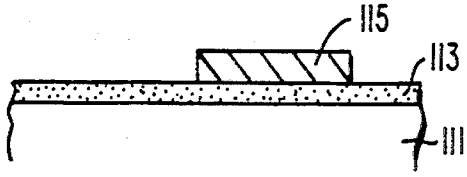


FIG._15.

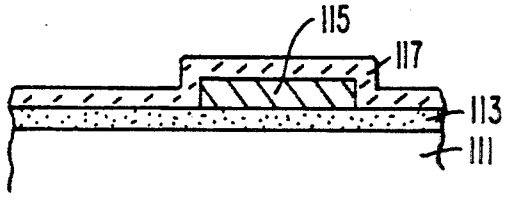


FIG._16.

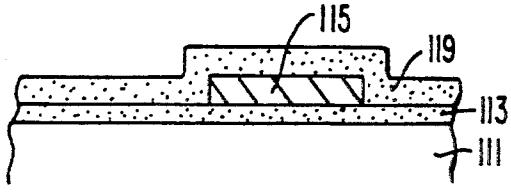


FIG._17.

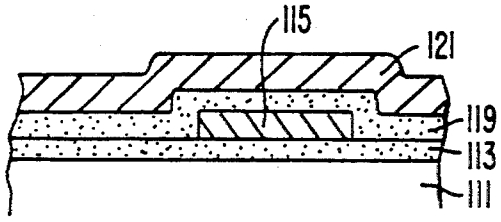


FIG._18.

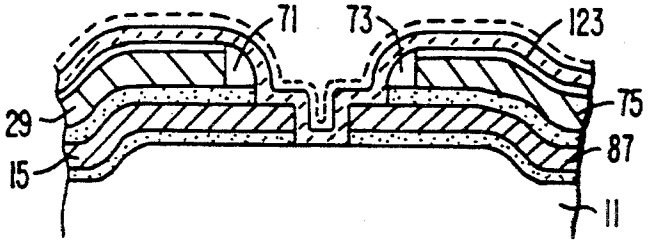


FIG._19.

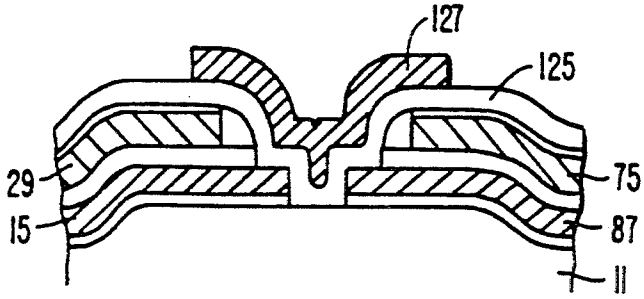


FIG._20.

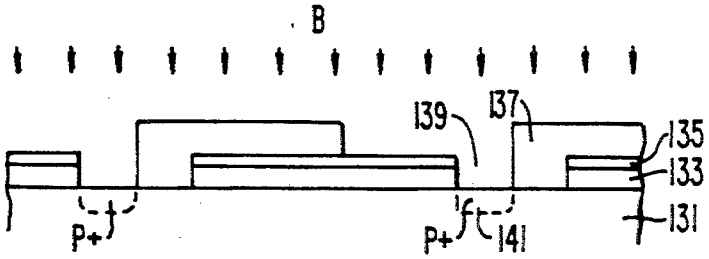


FIG._21.

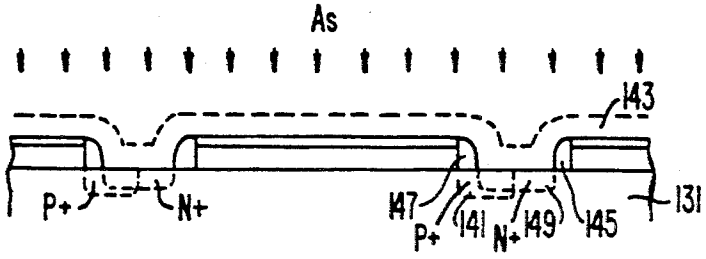


FIG._22.

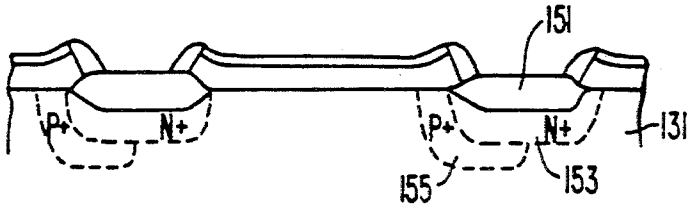


FIG._23.

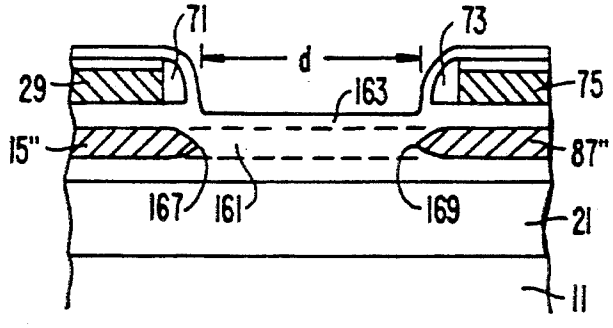


FIG._24.

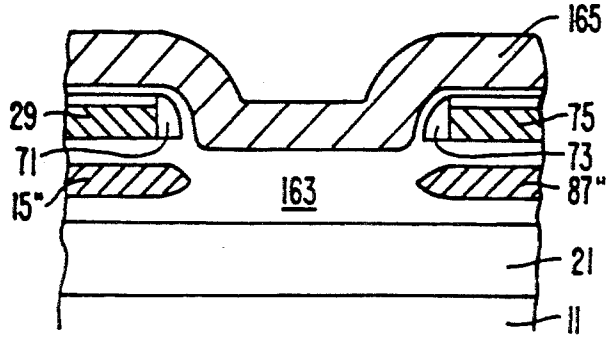


FIG._25.

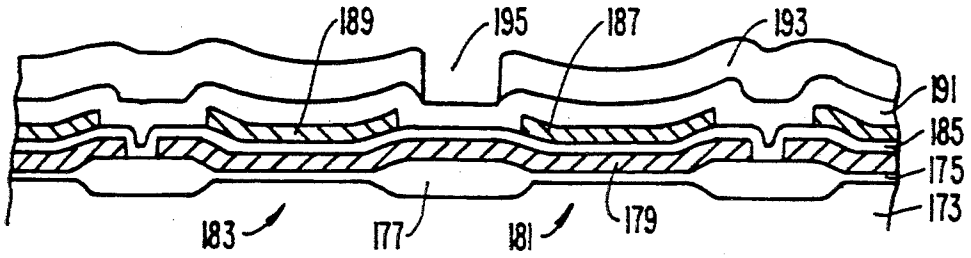


FIG._26.

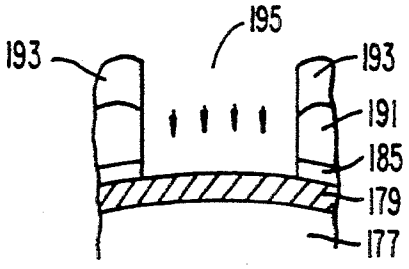


FIG._27.

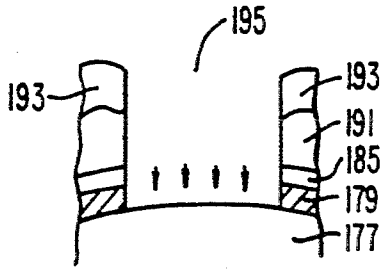


FIG._28.

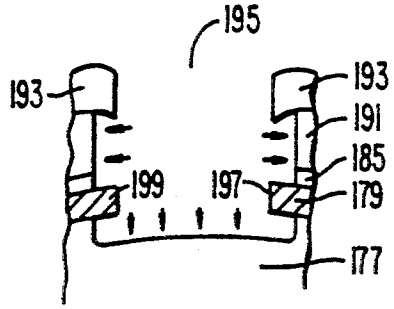


FIG._29.

METHOD OF MAKING DENSE FLASH EEPROM SEMICONDUCTOR MEMORY STRUCTURES

BACKGROUND OF THE INVENTION

This invention relates generally to semiconductor electrically erasable programmable read only memories (EEprom), and specifically to semiconductor structures of such memories and processes of making them.

An electrically programmable read only memory (Eprom) utilizes a floating (unconnected) conductive gate, in a field effect transistor structure, positioned over but insulated from a channel region in a semiconductor substrate, between source and drain regions. A control gate is then provided over the floating gate, but also insulated therefrom. The threshold voltage characteristic of the transistor is controlled by the amount of charge that is retained on the floating gate. That is, the minimum amount of voltage (threshold) that must be applied to the control gate before the transistor is turned "on" to permit conduction between its source and drain regions is controlled by the level of charge on the floating gate. The transistor is programmed to one of two states by accelerating electrons from the substrate channel region, through a thin gate dielectric and onto the floating gate.

The memory cell transistor's state is read by placing an operating voltage across its source and drain and on its control gate, and then detecting the level of current flowing between the source and drain. The level of current tells whether the device is programmed to be "on" or "off" at the control gate voltage selected. A specific, single cell in a two-dimensional array of Eprom cells is addressed for reading by application of a source-drain voltage to source and drain lines in a column containing the cell being addressed, and application of a control gate voltage to the control gates in a row containing the cell being addressed.

Early Eprom devices were erasable by exposure to ultraviolet light. More recently, the transistor cells have been made to be electrically erasable, and thus termed an electrically erasable and programmable read only memory (EEprom). Early EEprom cells were electrically erased by transfer of charge from the floating gate to the transistor drain through a very thin tunnel dielectric. This is accomplished by application of appropriate voltages to the transistor's source, drain and control gate. More recently, EEprom memory cells are provided with a separate, third gate for accomplishing the erasing. An erase gate passes through each memory cell transistor closely adjacent to a surface of the floating gate but insulated therefrom by a thin tunnel dielectric. Charge is then removed from the floating gate of a cell to the erase gate, when appropriate voltages are applied to all the transistor elements. An array of such EEprom cells are generally referred to as a Flash EEprom array because an entire array of cells, or significant group of cells, is erased simultaneously (i.e., in a flash).

Copending patent application Ser. No. 204,175 of Dr. Eliyahou Harari, filed June 8, 1988, contains a detailed discussion, with citations to the literature, of the prior art development of Eprom and EEprom devices in a section entitled "Detailed Description of the Prior Art," with respect to its FIGS. 1–4.

It is a primary object of the present invention to provide EEprom cell and array structures and processes

for making them that result in cells of reduced size so their density on a semiconductor chip can be increased.

It is also an object of the invention that the structures be highly manufacturable, reliable, scalable, repeatable and reproducible with a very high yield.

It is yet another object of the present invention to provide EEprom semiconductor chips that are useful as a solid state memory that can replace magnetic disk storage devices.

Another object of the present invention is to provide a process with an increased insensitivity to misalignment of masks used to manufacture the semiconductor devices.

Further, it is an object of the present invention to provide an EEprom structure capable of an increased number of program/read cycles that it can endure.

Additionally, it is an object of the present invention to provide an EEprom structure with a fast response to programming and/or erasing.

Another object of the invention is to provide improved semiconductor processing techniques and structures.

SUMMARY OF THE INVENTION

These and additional objects are accomplished by the various aspects of the present invention, the principal features of which will be briefly and generally summarized.

According to one aspect, opposing edges of control gates are used as a positional reference to define (mask) regions of the semiconductor structure between the control gates that are subjected to processing, such as by etching, deposition, implantation, oxide growth, and the like. A primary application is to define a region of underlying conductive strips that are removed in order to separate the strips into isolated floating gates. This region of the semiconductor structure is defined by at least one spacer of a controlled width being formed adjacent a control gate edge and extending partway toward an opposing control gate edge.

In a preferred form, a pair of spacers are formed on opposing edges of adjacent control gates to define a region in the middle for such processing. A preferred way of forming such spacers is to deposit a thick oxide layer over the semiconductor substrate and then remove it by reactive ion etching in a manner that leaves spacers adjacent the vertical edges of the control gate. The spacer width is controlled by the parameters of the etching and can be made to be very precise.

A primary advantage of this technique is that it is insensitive to the relative alignment of masks used in subsequent processing steps. Without having to allow for the tolerance of mask misalignment that occurs in every semiconductor process, the resulting memory circuit can be made with small dimensions and thus the density of memory cells on an integrated circuit can be increased.

An alternative technique for separating polysilicon strips into individual memory cell floating gates, according to another aspect of the present invention, is to open an aperture, in a photoresist or other type of mask, between two cells and remove a covering oxide layer and the polysilicon under it by an anisotropic etch. Following that, an isotropic etch for a controlled amount of time removes oxide from above and below edges of the separated polysilicon floating gates to expose a controlled area for subsequent growing of an erase dielectric layer thereover, followed by deposition

of an erase gate over the erase dielectric. This is an alternative technique that allows carefully defining the coupling area between the floating and erase gates in a manner that is reproducible.

With either of the techniques summarized above for masking the portion of the polysilicon strips to be removed in order to separate them into individual floating gates, an alternative to etching the polysilicon may be employed. According to a further aspect of the present invention, an oxide layer is grown on exposed portions of the polysilicon strips between the memory cells until the exposed polysilicon is completely consumed. This separates the polysilicon strips into floating gates of the adjacent memory cells. The floating gates are separated by a region that has been converted into a dielectric by oxidation, rather than by removing the polysilicon material through etching.

A further aspect of the present invention involves forming the floating gate somewhat differently than the control and erase gates, even though they all may be doped polysilicon material that is deposited by a chemical vapor deposition process. If the floating gate is so formed at a temperature of more than about 600–620 degrees Centigrade, its surface can be more effectively roughened by oxidation, to provide desired asperities in it, during the subsequent step of forming the erase dielectric over it. The surface asperities are desirable in order that the erase dielectric exhibit tunnel conduction of electrons through it from the floating gate to the erase gate during an erase cycle. It is desirable that the control and erase gates, on the other hand, be able to grow the highest quality dielectric with the lowest possible conduction through it. Therefore, the control and erase gates are preferably formed by the deposition process operating below 600–620 degrees Centigrade.

According to yet another aspect of the present invention, briefly and generally, an oxide layer of substantially uniform thickness is grown on a wafer being processed over exposed surfaces of material characterized by a significant differential rate of growth of oxide thereover. An example is a combination of exposed surfaces of lightly doped silicon and a doped polysilicon conductor, wherein oxide forms on the polysilicon at a higher rate than on the lightly doped silicon surface, often several times as fast, which results in an oxide layer being significantly thicker over the polysilicon than over the silicon. This is undesirable in certain applications. According to this invention, a uniform thickness layer of oxide is grown by first depositing over the exposed surfaces a layer of undoped polysilicon and then growing oxide over it until the polysilicon layer is substantially consumed by the oxidation process.

This oxidation technique has significant applications in the process of making Eprom and EEprom devices. One application is in forming the control gate oxide which extends over an oxide layer, previously formed directly on the semiconductor substrate surface, and polysilicon floating gate. Another application is in forming the erase gate oxide layer. A significant additional advantage of this technique in these applications is that a much purer oxide layer is formed over a doped polysilicon layer. When an oxide layer is grown directly over doped polysilicon in the usual manner, impurities are diffused into the grown oxide from the dopant in the underlying polysilicon. Since the intermediate polysilicon layer is undoped and the doped polysilicon layer is not oxidized, these impurities are substantially eliminated. The purer oxide layers, particularly the erase gate oxide, has a significant effect in extending the life of an EEprom in terms of the number of program/erase cycles it can endure before the number of electrons trapped in the oxide reach a level to render the EEprom substantially inoperable.

Yet another aspect of the present invention is a process for forming adjacent regions in the substrate surface which are ion implanted with dopants of opposite polarities. For example, in the EEprom devices described herein, a p-doped region is formed adjacent an n-doped source/drain region, both by ion implantation. Typically, both are currently implanted through a single opening in a mask and an inherent differential lateral diffusion is relied upon to position the p-doped region outside of and adjacent to the n-doped region. The process of the present invention, however, utilizes a spacer formed along at least one edge of the mask aperture during implantation of one polarity, with it being removed during implantation of the other polarity, in order to provide more control on the relative lateral positions of the two regions. The spacer protects the surface of the semiconductor substrate implanted with impurities of the first polarity type from overcompensation from the subsequent second implant of the opposite polarity.

Additional objects, features, and advantages of the various aspects of the present invention will become apparent from the following description of its preferred embodiments, which description should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic representation of an enlarged plan view of a plurality of electrically erasable and programmable read only memory cells formed on a semiconductor substrate in which the techniques of the present invention are utilized;

FIG. **2A** is a cross-sectional view of the memory array of FIG. **1**, taken at section A—A thereof;

FIG. **2B** is a cross-sectional view of the memory array of FIG. **1**, taken at section B—B thereof;

FIGS. **3A**, **4A**, **5A**, **6A**, and **7A** show in cross-sectional view several initial processing steps in the formation of the memory device of FIG. **1**, as viewed through section A—A thereof;

FIGS. **3B**, **4B**, **5B**, **6B**, and **7B** show in cross-sectional view several initial processing steps in the formation of the memory device of FIG. **1**, corresponding respectively to the views of FIGS. **3A**, **4A**, **5A**, **6A**, and **7A**, but viewed through section B—B of FIG. **1**;

FIGS. **8–12** illustrate later processing steps in forming the memory device of FIG. **1**, through section B—B thereof;

FIG. **13** is an enlarged view of completed adjacent memory cells of the memory circuit of FIG. **1**, taken across section B—B thereof;

FIG. **14** illustrates an equivalent electrical circuit of a single memory cell formed in accordance with the techniques of FIGS. **1–13**;

FIGS. **15–18** show sequential processing steps employed in an alternative technique for growing a layer of oxide;

FIGS. **19** and **20** illustrate a specific application of the technique shown by FIGS. **15–18**,

FIGS. **21–23** show sequential processing steps employed in an alternative technique for forming diffused regions in the substrate;

FIGS. 24 and 25 illustrate an alternative technique for separating a polysilicon strip into individual floating gates; and

FIGS. 26–29 show an alternative process for forming individual floating gates.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring initially to FIGS. 1, 2A, and 2B, principal elements of a completed multi-cell EEprom integrated circuit structure will be described. A substrate 11 is lightly p-doped and has individual memory cells formed on its surface 13. The structure of a single cell will be described since they are all the same. An electrically conductive, rectalinearly shaped floating gate 15, preferably made of polysilicon material, is formed on the substrate surface 13 on top of a thin, high-quality gate oxide 17 therebetween. Field oxide strips 19 and 21 isolate this cell from all others in the same column and from those in other columns.

Source/drain diffusions 23, 47 are formed under thick oxide strips 25, 26. Regions 23, 47 are heavily n-doped. An adjacent region 27 of relatively heavy p-doping is provided under the floating gate 15, extending from the source/drain diffusion 23.

An elongated control gate 29 passes across the floating gate 15 and is separated therefrom by a thin dielectric layer 31. On top of the control gate 29 is a thicker insulation layer 33, and insulating spacers 35 and 37 are provided along the edges of the control gate 29. Elongated erase gates 39 and 41 are insulated from the floating gate 15 by dielectric layers 43 and 45. The erase gates 39 and 41, and the control gate 29, are preferably made of a polysilicon conductive material, or a silicide or other refractory metal.

With reference primarily to FIG. 2, it can be seen that the EEprom example being described is of a split-channel type. That is, the floating gate 15 extends only partway across the channel 14 between the source/drain diffusion 23 and an adjacent source/drain diffusion 47. In a remaining portion of the channel 14, the control gate 29 is coupled to the substrate surface 13 through a thin gate oxide 49.

Use of Spacers To Form Floating Gates

An example process of forming the EEprom array illustrated in FIGS. 1, 2A and 2B, starts with an intermediate step illustrated in the sectional views of FIGS. 3A and 3B. FIG. 3A shows a stage of the construction of the device of FIGS. 1, 2A and 2B, across section A—A while the corresponding FIG. 3B shows the same stage of construction of the device as viewed across section B—B of FIG. 1. At the intermediate stage shown in FIGS. 3A and 3B, a nitride layer 51 has been formed on the surface 13 of semiconductor substrate 11 by ordinary techniques. Also by ordinary techniques, elongated, parallel openings 53 and 55 (FIG. 4A) have been formed in the nitride mask 51. Those openings have been restricted by photoresist portions 66 and 67, to leave openings 54 and 56. The elongated field oxide strips 19 and 21 have also been grown at this initial stage in the processing.

The step being performed in the illustration of FIGS. 3A and 3B is ion implantation with boron in order to form relatively heavily p-doped regions 61 and 63 coincident with the apertures 54 and 56, respectively. This is an initial series of steps in applying a standard DMOS process.

A next step, illustrated in FIGS. 4A and 4B, is to form heavily n-doped regions 57 and 59 in the substrate 11. The photoresist mask portions 66 and 67 are first removed in order to again open up apertures 53 and 55 in the nitride mask 51. Regions 57 and 59 are formed by ion implantation with arsenic.

A next step is to form thick oxide strips 25 and 65 by growing them over the diffusion strips, as illustrated in FIG. 5A. This thick oxide provides good insulation in the completed memory cell between the diffused regions and conductive gates that are formed later. It also allows etching to take place in subsequent steps without endangering the substrate.

Since this standard oxidation technique involves high temperatures, the implanted regions are diffused downward and laterally within the substrate 11, resulting in the enlarged heavily n-doped source/drain regions 23 and 62, and p-doped region 27, as an example in one cell, with lateral dimensions that are controllable. The diffusion rate of the p-dopant is higher than that of the n-dopant, resulting in relatively heavily p-doped regions 27 and 64 that extend laterally and in depth beyond the n-doped regions 23 and 62. The nitride mask layer 17 is then stripped off the wafer. As a next step, shown in FIGS. 5A and 5B, a thin, high-quality layer 17 of gate oxide is grown over the surface 13 of the semiconductor wafer 11.

A next step, illustrated in FIGS. 6A and 6B, is to form equally spaced conductive polysilicon strips, including strip 15′, which extends parallel to the diffusion strips and strips of oxide 25 and 65. A high quality layer 31′ of oxide is then grown over the entire wafer, a portion of which serves as the dielectric layer 31 between the floating and control gates.

A next step, illustrated in FIGS. 7A and 7B, is the formation of elongated, parallel strips of conductive polysilicon material to serve as the control gates for the memory cells. Control gate 29 is one of these. The elongated control gate strips are parallel to each other and oriented perpendicularly to the strips 15′ which will be processed to form the individual floating gates, discussed below. The control gates are formed with a thick oxide layer 33 deposited over them.

The process steps described so far will be recognized as a rather straight forward implementation of standard techniques which use a series of photographic masks to form protective masks on the wafer substrate surface in a pattern recorded on the photographic mask. Some process, such as etching, ion implantation or the like, is then accomplished through openings in the mask so formed on the wafer. Photoresist material is commonly used by coating it onto the wafer and exposing to the light pattern of the photographic mask. The photoresist volume that is exposed to light has a different solubility than the surrounding, unexposed volume, allowing a portion to be differentially removed by washing in an appropriate solution.

A problem always exists in aligning photographic masks so that the sequential steps build on one another in the proper way. Very sophisticated techniques have been developed for registering each new photographic mask to the pattern previously formed on the semiconductor wafer by use of prior photographic masks. However, there is a limit as to how accurately such registration can be accomplished. As semiconductor devices become more dense, the resolution requirements for patterns used in forming them have increased greatly, to the point where the ability to register subsequent photo-

graphic masks with each other is a limitation as to how close various parts of semiconductor structure being formed can be placed. Therefore, the process being described has been carefully designed in order to obtain a very high resolution structure that is not limited by tolerances inherent in current mask alignment techniques.

As an example of what has been described previously, the relatively heavy p-doped region **27** in the substrate is formed to be an active area for electron transfer to the floating gate **15**. The threshold voltage that can be programmed into the cell is thus not so dependent upon the alignment of the floating gate **15** with respect to its source/drain diffusion **23**. That is, the amount of the channel region between adjacent source/drain regions **23** and **62** that is covered by the floating gate **15** is not so critical as it is when the enhanced region **27** is not utilized. The width of the region **27** at the wafer surface **13** is controlled by lateral diffusion after ion implantation in accordance with FIG. **3A**. The amount of lateral diffusion can be carefully controlled so that the alignment of the mask used to form the photoresist strips **66** and **67** in FIG. **3A** is not highly critical to the resultant forming the lateral extent of the p-doped region **27** which affects the operation of the device.

A next major processing step after that described with respect to FIGS. **7A** and **7B** is illustrated in FIG. **8**, a section taken through B—B of FIG. **1**. The steps illustrated in FIG. **8** have a goal of forming spacers along opposing edges of parallel control gates, such as the spacers **71** and **73** formed along opposing edges of adjacent control gate strips **29** and **75**. The spacers are formed by depositing a thick layer **77** of undoped silicon dioxide over the entire chip, and then removing most of it by a dry reactive ion etching process. This process etches layer **77** in a vertical direction only, thereby leaving the spacers **71** and **73**. The spacers are formed in a region of the layer **77** against the edges of the control gates **29** and **75** where the layer **77** is thicker than elsewhere. The dry etch is continued for a time to result in the spacers having a desired width. This width can be controlled very precisely by this process At the same time, the portion of the oxide layer **31'** between the spacers will be removed, thereby leaving the oxide layer **31** and oxide layer **79** under the adjacent control gates **29** and **75**. The etch is stopped before the oxide layers **33** on top of the control gates are reduced below their desired thickness.

A next step is to densify the spacers by raising the temperature of the wafer in excess of 800° C. A second pair of spacers **81** and **83** (FIG. **9**) is then formed in a similar manner. A layer **85** of phosphorous-doped or boron-phosphorous-doped silicon dioxide is deposited over the entire wafer and then removed by a dry reactive ion etch with parameters selected to leave the second spacers **81** and **83** with a desired width. As mentioned previously, this process is capable of forming such spacers with a desired width, within a very few percent.

The purpose of the double spacers is to form a gap between them, indicated by the distance "d", as an opening for etching through the elongated polysilicon strip **15'** in order to separate it into individual, isolated floating gates, such as the adjacent gates **15** and **87** shown in FIG. **10**. The spacers serve as a mask to protect the edges of the desired floating gates from attack by the etching process. An appropriate reactive ion etch or plasma etch may be used to form a gap **89** between adjacent floating gates It will be noted that this gap has been formed without reliance upon alignment of successive photographic masks. The distance between opposing edges of adjacent control gates, such as control gates **29** and **75**, are fixed by the photographic mask used to form those polysilicon strips. By using opposing edges of the control gates as a reference from which to define the gap "d" to be formed in the underlying floating gate strip **15'**, the tolerance that must be allowed for misalignment of successive photographic masks is not a limitation as to how small the distance "d" can be made. As a result, the individual EEprom memory cells are packed closer together in the dimension illustrated in FIGS. **8-12**.

In order to provide an exposed surface on adjacent edges of each of the floating gates **15** and **87** that may be coupled to an erase gate, the most recently formed spacers, such as spacers **81** and **83**, are removed by an appropriate wet etch. Because the first set of spacers **71** and **73**, and all other exposed oxide, was densified prior to forming the second spacers **81** and **83**, the spacers **81** and **83** will be etched at a much higher rate than any of the other exposed oxide. Indeed, the doped oxide spacers **81** and **83** are typically etched at a rate that is at least 50–100 times faster than that of the densified undoped oxide.

As shown in FIG. **11**, opposing edges of adjacent floating gates **15** and **87** have erase gate oxide layers **45** and **93** grown over them. Indeed, the process grows such a layer over most of the integrated circuit chip but it is important only in the areas indicated at **45** and **93**. Additionally, the oxide is grown at a much faster rate over the polysilicon material of the floating gates **15** and **87** than it is over the exposed oxide that exists in most of the remaining portion of the wafer.

As indicated in FIG. **12**, the erase gate **41** is formed, either from a metal such a aluminum or polysilicon, in a manner where the erase oxide layers **45** and **93** separate the erase gate **41** from adjacent floating gates **15** and **87**.

The techniques described above represent an improved way of self-aligning the floating and control gates of the EEprom embodiment illustrated in FIGS. **8*a*** and **8*b*** of the aforementioned patent application Ser. No. 204,175. A significant advantage of this process is that the erase oxide layers **45** and **93** are formed independent of any other operation. That is, the erase oxide is not formed as part of the same layer as some other oxide, such as that between the floating and control gates, as in other processes. As a result, the coupling between the floating and erase gates can be optimized. A tunneling dielectric layer is preferred and it is made very thin, which results in a lower voltage needing to be applied across the erase oxide layers when the floating gates are being erased. This has the advantage of prolonging the number of erase cycles that can be accomplished before the erase oxide begins to deteriorate. It also shortens the time necessary to accomplish a full erase. The process also allows forming asperities on the exposed portions of the floating gates by oxidation followed by etching without affecting other surface portions of the floating gates, before forming the oxide layers **45** and **93**, thereby to further enhance the erase characteristics of the device without introducing undesired side effects.

Referring to FIG. **13**, some dimensions are indicated. The amount of area of each floating gate **15** and **87** that is coupled to their common erase gate **41** includes the vertical edges of the floating gate and the surface area

having a dimension S'. The dimension S' is controlled primarily by the width of the second spacers **81** and **83** used in the process. The process assures that the coupling with each floating gate and its associated erase gate is substantially the same, a coupling that is controlled by the distance S', the thickness and composition of the erase dielectric layers **45** and **93**, and the surface roughness of the floating gate. The distance S is controlled by the sum of the widths of the two spacers utilized. It is desired that the thickness of the spacers **71** and **73** be sufficient to result in little or no coupling between adjacent control gates **29** and **75** and the erase gate **41**. Similarly, oxide layers **33** and **95** are maintained thick enough for the same desired isolation.

The structure of FIG. **2B** implies that erase gates **39**, **41** are provided at the two erase dielectric regions **43**, **45** of each floating gate **15**. However, it is possible to have only one of the two regions of erase dielectric covered by an erase gate.

FIG. **14** is an equivalent circuit that generally illustrates the coupling between the three conductive gates of a single EEprom cell. A capacitance **101** shown in dotted outline indicates practically no coupling between the erase gate **41** and the control gate **15**. These elements are uncoupled, as explained above, by the spacer **71** and thick oxide layer **33** on top of the control gate **29**. Coupling between the erase gate **41** and floating gate **29** is indicated as a relatively small capacitance **103**. The coupling between the floating gate **29** and the control gate **15**, on the other hand, is indicated by a relatively large capacitance **105**. The capacitances **103** and **105** are controlled primarily by the thickness of the dielectric between the elements and the extent of the common area between the adjacent gate elements.

The advantages of controlling the coupling in this manner can be explained with respect to FIG. **14** for an erase cycle, where a voltage such as 20 volts is placed on the erase gate and the control gate is held at ground potential. The combination of the relatively close coupling between the control gate and floating gate (indicated by the large capacitance **105**) and the relatively low degree of coupling between the erase gate and floating gate (indicated by the small capacitance **103**) causes the floating gate to be held close in voltage to the control gate. That results in a large voltage difference between the erase gate and floating gate, and thus a strong electric field that tends to move electrons from the floating gate to the erase gate. A significant advantage of this is that the floating gate can be erased more easily and quickly. It even allows reducing the erase gate voltage, which then increases the life of the device and makes the design of surrounding circuits easier.

When a cell is being programmed, the voltages are reversed, the control gate being held at about 12 volts, the erase gate is held at 0 volts, the drain at 8 volts and the source is held at ground potential. Because of the close coupling between the floating and control gates, the voltage on the control gate more significantly enhances the injection of electrons onto the floating gate from the device substrate. The low degree of coupling between the erase and floating gates reduces the undesirable interaction between those two elements during a programming cycle.

The doped polysilicon layers are preferably formed by a chemical vapor deposition process. Since it is important that the edges of the floating gate interface with the erase gates be roughened to leave asperities in their surfaces, the floating gates must be formed in a manner that allows such roughening to be accomplished during the formation of the erase dielectric layer. It is much easier to do so if the floating gates are deposited by a low pressure chemical vapor deposition process at a deposition temperature in excess of 600°-620° C. By doing so at this high temperature, the formation of asperities during the subsequent oxidation to grow the erase oxide is greatly enhanced, resulting in an erase dielectric which exhibits greatly enhanced tunnel conduction during erase of the floating gates. In order to allow formation of the highest quality (i.e. lowest conduction) oxide layer on the control and erase gates, formation of asperities should be suppressed on their surfaces. To achieve this condition concurrent with the enhanced conductivity of the erase oxide, those gates are formed by a chemical vapor deposition process at a deposition temperature of less than 600° C.

Process of Forming Thin Oxide Layers

As can be seen from FIG. 7A, the oxide layer **31'** is grown over surfaces of different materials. One material is the lightly doped silicon substrate layer **13**, and the other material is heavily doped polysilicon layer **15'**. As is well known, the rate of growth of oxide on such heavily doped polysilicon is much higher, in a range of from 1.5 to 5 times as high, as that grown over the lightly doped silicon **13**. Therefore, it can be difficult to make the oxide layer **31'** thin enough over the polysilicon strip **15'** in order to serve as a good gate oxide layer between the floating and control gates, without resulting in the gate oxide **49** between the control gate and the substrate from being thinner than desired.

Also, it is desired that the oxide layers grown over the doped polysilicon conductive material be as high a quality as possible. Some of the dopant within the polysilicon material, typically phosphorus, is retained in an oxide layer grown over the polysilicon during the usual thermal oxidation techniques. This impurity is undesirable in many of the thin oxides so grown, particularly for the erase oxides, such as the layers **45** and **93**, which are grown over the edges of floating gates, such as the floating gates **15** and **87**. It is believed that these impurities contribute to trapping electrons in the erase oxide layers over time, thus significantly contributing to the existing limitation of the number of program/erase cycles through which a memory cell may be put before it can no longer be effectively erased.

In order to overcome the foregoing disadvantages of directly growing an oxide layer over undoped as well as doped polysilicon conductive layers, a thin layer of undoped polysilicon is first deposited and then oxide grown thereover at a relatively low temperature (between 800°-900° C.) until substantially the entire undoped polysilicon material layer has been consumed and made part of the grown oxide layer. This technique results in a uniform thickness of oxide being formed over both lightly doped and heavily doped polysilicon surfaces, and is significantly purer since the doped polysilicon material is not made part of the oxidation process.

Referring to FIG. **15**, this technique is illustrated for a semiconductor wafer **111** having a thin oxide layer **113** thereover and a phosphorus doped polysilicon layer **115** over a portion of the oxide layer's **113** surface. FIG. **16** shows a layer **117** of undoped polysilicon having been deposited by a chemical vapor deposition process with an uniform thickness over both the oxide and

polysilicon layers. This thickness depends upon the desired ultimate thickness of the oxide layer.

A next step, shown in FIG. **17**, is to form an oxide layer over the undoped polysilicon layer **117** until, as a result, substantially the entire amount of undoped polysilicon has been consumed. An oxide layer **119** is the result, having a thickness that is greater than that of the undoped polysilicon layer **117** by a known amount. An additional step that may be desired in certain circumstances is to first grow a very thin layer of barrier oxide over the initially exposed surfaces of FIG. **15** before the undoped polysilicon layer **117** (FIG. **16**) is deposited over it. This assures that the phosphorus or other impurities in the polysilicon layer **115** will not end up in the oxide layer **119** because the oxidation proceeds beyond the point that all of the undoped polysilicon layer **117** is consumed If the oxidation does proceed too far, without such a barrier layer, a low level of impurities in the doped polysilicon layer **115** can become part of the oxide layer as the polysilicon **115** is consumed by the oxidation process.

The polysilicon layer **115** is representative of a floating gate in the EEprom processing embodiments described above. After the oxide layer **119** of uniform thickness is formed, another doped polysilicon layer **121** is deposited over it to serve as a control gate (FIG. **18**).

FIG. **19** illustrates the process described with respect to FIGS. **15–18** being applied to form the erase gate oxide. FIG. **19** corresponds to FIG. **11** before its erase oxide layers **45** and **93** are formed. Rather than oxidizing the exposed edges of the floating gates **15** and **87** directly, as is done in the embodiment of FIG. **11**, a layer **123** of undoped polysilicon is deposited over the entire surface, in a manner described previously. This polysilicon layer, if sufficiently thin (i.e. 500 Angstrom or less), follows the asperities in the surface of the exposed floating gate edges. The layer **123** then has an oxide layer grown over it until it is substantially entirely consumed, at which time it is converted into a thicker oxide layer **125**, as shown in FIG. **20**. An erase gate **127** is then formed over the oxide layer **125**, resulting in higher quality erase oxide between the erase gate **127** and edges of the floating gates **15** and **87**.

Process of Forming Diffused Regions

FIGS. **21–23** show several process steps, as an for forming the heavily n-doped source/drain regions and relatively heavily p-doped channel region. The process illustrated in FIGS. **21–23** is also an improvement over that illustrated in the process steps of FIG. **14** of the aforementioned patent application Ser. No. 204,117.

Referring to FIG. **21**, a semiconductor substrate **131** has a nitride mask layer **133** with an etch stop thin oxide layer **135** over it. Openings in the nitride mask **133** are partially, temporarily covered by photoresist material **137** in order to form a restricted opening **139**. A relatively heavily p-doped region **141** is formed in the substrate by ion implantation of boron through the opening **139**. So far, the process is much the same as that described earlier with respect to FIGS. **3A** and **3B**.

However, as shown in FIG. **22**, instead of performing the next implantation step through the entire width of the apertures in the nitride mask **133**, those apertures are first restricted in width. This is accomplished by depositing a nitride layer **143** over the structure, after the photoresist layer **137** has been removed. The layer **143** is then etched by an anisotropic reactive ion etch process in a manner to leave spacers **145** and **147** along the edges of the nitride mask **133** at its openings The relatively heavily n-doped region **149** is then formed in the substrate **141** by ion implantation of arsenic. It will be noted that the heavily p-doped region **141** is laterally displaced from an edge of the heavily n-doped region **149**, before those regions are diffused into the wafer by heating. Thus, the position and size of the region **141** can be better controlled, without having to rely entirely on the inherent differential diffusion rate of the p- and n-regions, as with the process of FIGS. **3–5**. (Relatively heavily doped region **141** is typically a doping concentration of around 1×10^{17} cm^{-3} while heavily doped region **149** is typically of doping concentration of around 1×10^{20} cm^{-3}). The spacer **147** protects the surface of the substrate **131** under it, which has been implanted with impurities of a first polarity, from being overcompensated during the step of implanting impurities of a second polarity.

FIG. **23** shows a next step of growing a thick oxide layer **151** in the surface of the silicon substrate **131** in the openings in the nitride mask **133** between the spacers **145** and **147**. At the same time, the heating causes expansion of the implanted regions, resulting in a heavy n-type region **153** and a relatively heavy p-type region **155**. By oxidizing through the aperture restricted by the spacers **145** and **147**, the width of the thick oxide **151** is smaller than before, thus allowing a smaller device to be constructed. After the process step illustrated in FIG. **23** is accomplished, the nitride mask **133** is removed and processing continues as previously described with respect to FIGS. **6–12**.

Alternate Technique for Forming Floating Gates

In the process previously described, a continuous conductive polysilicon strip was separated into individual floating gates by an etching process, as described with respect to FIGS. **9** and **10**. An alternate technique that has some advantages in certain circumstances is explained with respect to FIGS. **24** and **25**. Instead of etching the polysilicon strip into its individual floating gates, oxide is grown over exposed polysilicon until the entire thickness of the polysilicon is consumed by the oxidation process.

Referring to FIG. **24**, an enlarged representation of FIGS. **9** and **10** is provided, with the same reference numbers applied to those elements which are the same. The continuous doped polysilicon strip is separated into adjoining floating gates 15″ and 87″ by oxidizing the polysilicon strip exposed between the spacers **71** and **73** until its portion **161** is totally consumed by the oxidation process. The result is an oxide layer **163**, over which a conductive layer **165** may be formed as the erase gate.

A result of this technique is the shaping of edges of the floating gates to a narrow line or point, such as that indicated at **167** and **169**. This point aids in proper coupling between the floating gates and the erase gate on the opposite side of the erase gate being formed. This is an improved technique for forming the pointed floating gate illustrated in FIG. **16***b* of the aforementioned patent application Ser. No. 204,175.

In addition to the advantage of the resulting pointed floating gate edges, the process described with respect to FIGS. **24** and **25** also allows the thick oxide layer **21** to be made thinner, and perhaps even eliminated completely, since the etching of the polysilicon to form floating gates (which may also result in etching of any areas of exposed silicon substrate **11**) is replaced by an oxidation step.

Mask Formation of Floating Gate Edges

As an alternative to the embodiment described with respect to FIGS. 8–12, FIGS. 26–29 illustrate another sequence of processing steps. Referring initially to FIG. 26, a substrate 173 has formed on its surface an oxide layer 175 with alternate thin and thick stripes thereacross, including a thick oxide portion 177. Immediately on top of this oxide layer is a strip 179 of conductive polysilicon material that is to be formed into individual floating gates. Rather than initially extending this strip substantially completely across an array of many memory cells, the doped polysilicon strip 129 is formed by a mask that limits its length to extend across only two adjacent memory cells being formed, in this case cells 181 and 83. A subsequent series of processing steps, to be described, then separate the strip 179 into two individual, adjacent floating gates with an erase gate between them and coupled with both.

The starting structure of FIG. 26 also includes a thin control gate oxide layer 185, and a series of parallel control gate strips extending with their length and their direction perpendicular to the paper, such as control gates 187 and 189 for the cells 181 and 183, respectively. On top of the control gates, and the rest of the structure is then formed an oxide layer 191. The structure thus described with respect to FIG. 26 is similar to that of FIG. 7B, in the prior embodiment, with the primary difference that the polysilicon strip which is to be used to form individual floating gates extends across only two adjacent memory cells.

In order to separate the strip 179 into two floating gate portions, a photoresist mask 193 is formed on top of the structure with an opening 195 therein positioned by a photographic mask. Three different etching steps are then performed in sequence to operate on the structure that is accessible through the opening 195. The first of these etching steps, illustrated in FIG. 27 is an anisotropic dry etch of the oxide layer 185, 191. Of course, the opening in the oxide layer then conforms substantially to that of the opening 195 in the photoresist layer 193. The second etch, illustrated by FIG. 28 is an anisotropic etch of the polysilicon layer 179 to separate it into floating gates for the adjacent memory cells 181 and 183 that are separated from each other. The type of etch employed selectively operates upon the doped polysilicon material at a much faster rate than on oxide, so the exposed oxide layers are substantially unaffected.

The third of the etching steps is illustrated in FIG. 29, and is a short isotropic wet etch that moves the sidewalls of the exposed oxide layer 191, 185 back under the photoresist 193. At the same time, the thick field oxide portion 177 is vertically etched and laterally etched under the floating gates. The result is the clean exposure of edges 197 and 199 of adjacent floating gates.

Once these floating gate edges are exposed, the photoresist material 193 is removed and an erase gate oxide layer is grown on the exposed floating gate portions 197 and 199, in a manner described previously with respect to other embodiments. After that, an erase gate is formed by depositing conductive material, usually doped polysilicon, in the opening formed by the etch and isolated from the floating gate edges 197 and 199 by only the grown erase gate oxide. Because the isotropic wet etch step illustrated in FIG. 29 allows good control of the amount of the floating gate edges 197 and 199 that are exposed, the area of coupling between these floating gates and the subsequently formed erase gate can be carefully controlled. Because of this control, erase gates need not be provided on opposite sides of each floating gate, as done in other EEprom processes as compensation for potential misalignment between the erase gates and the floating gates within the tolerance of photographic mask alignment. Indeed, although two erase gates are shown coupled to each of the floating gates in the embodiment described with respect to FIGS. 1–14, the good control of coupling area between its floating gates and erase gates also allow every other erase gate shown in those figures to be eliminated, if desired.

In the process embodiment of FIGS. 26–29, the exposed polysilicon floating gate material is etched away. However, the process there described can be altered to separate the polysilicon strip 179 into two floating gates by the oxidation process earlier described with respect to FIGS. 24 and 25.

Although the various aspects of the present invention have been described with respect to its preferred embodiments, it will be understood that the invention is entitled to protection within the full scope of the appended claims.

It is claimed:

1. A method of forming a two dimensional array of flash electrically erasable and programmable read only memory cells on a semiconductor substrate, comprising the steps of:

forming a first plurality of continuous elongated parallel strips of conductive material on said substrate in a manner to be insulated therefrom by a first dielectric layer,

forming a second plurality of continuous elongated parallel strips of conductive material on said substrate and over said first plurality of conductive strips in a manner to be insulated therefrom by a second dielectric layer, said first and second plurality of strips having their lengths oriented substantially orthogonal to each other,

thereafter forming spacers along opposing edges of adjacent ones of said second plurality of parallel strips and extending toward each other but leaving a defined space therebetween, and

thereafter forming a gap in said first plurality of strips through the space defined by the spacers, thereby forming electrically isolated floating gates from said first plurality of strips.

2. The method according to claim 1 wherein the step of forming a gap in said first plurality of strips includes applying an etchant to said first plurality of strips in a region defined by said spacers.

3. The method according to claim 1 wherein the step of forming a gap in said first plurality of strips includes the step of oxidizing said first plurality of strips in a region defined by said spacers.

4. The method according to claim 1 which additionally comprises, after the first conductive strips have been separated into electrically isolated floating gates, the additional steps of forming asperities adjacent edges of said floating gates, and forming a third dielectric layer thereover.

5. The method according to claim 3 wherein the step of forming a dielectric of said floating gates includes:

forming a layer of an undoped polysilicon material of a substantially uniform thickness across said semiconductor structure, and

thereafter growing a layer of oxide on the undoped polysilicon material layer for a time until substantially the entire undoped polysilicon material layer

has been consumed and made part of the grown oxide layer.

6. The method according to claim 1 wherein said second dielectric layer is formed by the steps of:

forming a layer of an undoped polysilicon material of a substantially uniform thickness across said semiconductor structure, and

thereafter growing a layer of oxide on the undoped polysilicon material layer for a time until substantially the entire undoped polysilicon material layer has been consumed and made part of the grown oxide layer.

7. A method of forming a two dimensional array of flash electrically erasable and programmable read only memory cells on a semiconductor substrate, comprising the steps of:

forming a first plurality of continuous elongated parallel strips of conductive material on said substrate in a manner to be insulated therefrom by a first dielectric layer, including depositing doped polysilicon by low pressure chemical vapor deposition at a temperature in excess of 620 degrees centigrade,

forming a second plurality of continuous elongated parallel strips of conductive material on said substrate and over said first plurality of conductive strips in a manner to be insulated therefrom by a second dielectric layer, said first and second plurality of strips having their lengths oriented substantially orthogonal to each other, wherein the step of forming the second plurality of elongated strips includes depositing doped polysilicon by low pressure chemical vapor deposition at a temperature less than 600 degrees centigrade,

thereafter forming spacers along opposing edges of adjacent ones of said second plurality of parallel strips and extending toward each other but leaving a defined space therebetween, and

thereafter performing an operation on said first plurality of strips through the space defined by the spacers.

8. A method of forming a two dimensional array of flash electrically erasable and programmable read only memory cells on a semiconductor substrate, comprising the steps of:

(a) implanting dopant of opposite polarity in adjacent regions of a semiconductor substrate, by a method comprising the steps of:

forming a first masking layer over said substrate which has a plurality of apertures therein,

providing a second mask over said first masking layer in a manner to cover a portion of said apertures from one side thereof, thereby leaving a first restricted opening to said substrate adjacent an opposite side of said apertures,

performing a first implant of impurities of a first polarity through said first restricted opening, removing said second mask while maintaining said first masking layer in place,

forming a spacer within said apertures at least along said opposite side thereof, thereby forming a second restricted opening therethrough, and providing a second implant of a second polarity opposite to said first polarity through said second restricted opening,

whereby said spacer protects the surface of said semiconductor substrate which is implanted with impurities of the first polarity from over compensation from the second implant of said opposite polarity,

(b) thereafter forming a first plurality of continuous elongated parallel strips of conductive material on said substrate in a manner to be insulated therefrom by a first dielectric layer,

(c) thereafter forming a second plurality of continuous elongated parallel strips of conductive material on said substrate and over said first plurality of conductive strips in a manner to be insulated therefrom by a second dielectric layer, said first and second plurality of strips having their lengths oriented substantially orthogonal to each other,

(d) thereafter forming spacers along opposing edges of adjacent ones of said second plurality of parallel strips and extending toward each other but leaving a defined space therebetween, and

(e) thereafter performing an operation on said first plurality of strips through the space defined by the spacers.

9. A method of forming a two dimensional array of flash electrically erasable and programmable read only memory cells on a semiconductor substrate, comprising the steps of:

forming a first plurality of elongated parallel strips of conductive material on said substrate in a manner to be insulated therefrom by a first dielectric layer,

forming a second plurality of elongated parallel strips of conductive material on said substrate and over said first plurality of conductive strips in a manner to be insulated therefrom by a second dielectric layer, said first and second plurality of strips having their lengths oriented substantially orthogonal to each other, thereby to form control gates,

forming spacers of dielectric material along opposing edges of said control gates and extending toward each other with a gap of a predetermined width remaining therebetween that exposes portions of said first plurality of strips therein,

etching away said exposed portions of said first plurality of strips, thereby forming isolated floating gates extending between etched spaces therebetween,

thereafter reducing the size of the spacers in a manner to expand said gap, thereby exposing surface area portions of said floating gates adjacent said spacers,

forming a third dielectric layer over the exposed surface area of the floating gates, and

forming a third plurality of elongated parallel strips of conductive material across said third dielectric, thereby to form erase gates.

10. A method of forming a two dimensional array of flash electrically erasable and programmable read only memory cells on a semiconductor substrate, comprising the steps of:

forming a first plurality of elongated parallel strips of conductive material on said substrate in a manner to be insulated therefrom by a first dielectric layer,

forming a second plurality of elongated parallel strips of conductive material on said substrate and over said first plurality of conductive strips in a manner to be insulated therefrom by a second dielectric layer, said first and second plurality of strips having their lengths oriented substantially orthogonal to each other, thereby to form control gates,

forming spacers of dielectric material along opposing edges of said control gates and extending toward each other with a gap of a predetermined width

remaining therebetween that exposes portions of said first plurality of strips therein, said spacer forming step including forming first and second spacer portions in time sequence adjacent each other, the material of said first spacer portion exhibiting a significantly slower response to a given etching process than the material of said second spacer portion,

etching away said exposed portions of said first plurality of strips, thereby forming isolated floating gates extending between etched spaces therebetween,

thereafter reducing the size of the spacers in a manner to expand said gap, thereby exposing surface area portions of said floating gates adjacent said spacers, said spacer reducing step including the step of removing said second spacer portion by said given etching process,

forming a third dielectric layer over the exposed surface area of the floating gates, and

forming a third plurality of elongated parallel strips of conductive material across said third dielectric, thereby to form erase gates.

11. The method according to claim **10** wherein said first spacer portion is formed of densified undoped silicon dioxide, said second spacer portion is formed of silicon dioxide doped with phosphorus, and said given etching process is a wet etch.

12. The method according to claim **9** wherein the step of forming the spacers includes forming a single spacer portion, and further wherein the step of reducing the size of the spacers includes the step of etching said single spacer portion in a manner to reduce its size.

13. A method of forming a two dimensional array of flash electrically erasable and programmable read only memory cells on a semiconductor substrate, comprising the steps of:

forming a first plurality of elongated parallel strips of conductive material on said substrate in a manner to be insulated therefrom by a first dielectric layer,

forming a second plurality of elongated parallel strips of conductive material on said substrate and over said first plurality of conductive strips in a manner to be insulated therefrom by a second dielectric layer, said first and second plurality of strips having their lengths oriented substantially orthogonal to each other, thereby to form control gates,

forming spacers of dielectric material along opposing edges of said control gates and extending toward each other with a gap of a predetermined width remaining therebetween that exposes portions of said first plurality of strips therein,

etching away said exposed portions of said first plurality of strips, thereby forming isolated floating gates extending between etched spaces therebetween,

thereafter reducing the size of the spacers in a manner to expand said gap, thereby exposing surface area portions of said floating gates adjacent said spacers,

forming a third dielectric layer over the exposed surface area of the floating gates,

forming a third plurality of elongated parallel strips of conductive material across said third dielectric, thereby to form erase gates, and

forming a fourth layer of dielectric over the control gates before the erase gates are formed, thereby isolating said control and erase gates.

14. The method according to claim **13** wherein said second, third and fourth dielectric layers are formed in separate steps, whereby each of these dielectric layers may be optimized to perform specific functions required of it.

15. The method according to claim **9** wherein the step of forming a third plurality of elongated strips of conductive material includes forming them in a direction substantially parallel to said control gates.

16. A method of forming a two dimensional array of flash electrically erasable and programmable read only memory cells on a semiconductor substrate, comprising the steps of:

forming a first plurality of elongated parallel strips of conductive material on said substrate in a manner to be insulated therefrom by a first dielectric layer, including depositing doped polysilicon by low pressure chemical vapor deposition at a temperature in excess of 620 degrees centigrade,

forming a second plurality of elongated parallel strips of conductive material on said substrate and over said first plurality of conductive strips in a manner to be insulated therefrom by a second dielectric layer, said first and second plurality of strips having their lengths oriented substantially orthogonal to each other, thereby to form control gates, wherein the step of forming the second plurality of elongated strips includes depositing doped polysilicon by low pressure chemical vapor deposition at a temperature less than 600 degrees centigrade,

forming spacers of dielectric material along opposing edges of said control gates and extending toward each other with a gap of a predetermined width remaining therebetween that exposes portions of said first plurality of strips therein,

etching away said exposed portions of said first plurality of strips, thereby forming isolated floating gates extending between etched spaces therebetween,

thereafter reducing the size of the spacers in a manner to expand said gap, thereby exposing surface area portions of said floating gates adjacent said spacers,

forming a third dielectric layer over the exposes surface area of the floating gates, and

forming a third plurality of elongated parallel strips of conductive material across said third dielectric, thereby to form erase gates.

17. A method of forming a plurality of flash electrically erasable and programmable read only memory cells on a semiconductor substrate, comprising the steps of:

forming a first layer of doped polysilicon conductive material across two adjacent of said memory cells and insulated from said substrate by first dielectric layer,

forming a second dielectric layer over said first polysilicon layer,

forming a second layer of doped polysilicon conductive material as a control gate over each of said adjacent memory cells,

forming a third dielectric layer across said control gate and exposed portions of said second dielectric layer therebetween,

forming a mask over said third dielectric layer with an aperture therein positioned between the adjacent cells but over the first polysilicon layer extending therebetween,

removing the third dielectric layer and said first doped polysilicon layer under the aperture of said photoresist mask by subjecting them to an anisotropic etch, thereby separating the first doped polysilicon layer into a separate floating gate for each of said at least two adjacent cells and to leave a well in the structure under said aperture,

thereafter partially etching said third dielectric layer exposed through said photoresist mask aperture by an isotropic etch, thereby moving vertical dielectric walls away from the region under said photoresist aperture to leave edges of the separated first doped polysilicon layer extending beyond said vertical dielectric walls and into said well,

stripping said mask from said third dielectric layer,

forming a fourth dielectric layer over the exposed polysilicon floating gates in said well, and

forming an erase gate in said well in a manner that the fourth dielectric layer separates said erase gate from each of the separated first polysilicon layer floating gates.

18. The method according to claim **17** wherein any of said first, second or fourth dielectric layers is formed by the steps of:

forming a layer of an undoped polysilicon material of a substantially uniform thickness across said semiconductor structure, and

thereafter growing a layer of oxide on the undoped polysilicon material layer for a time until substantially the entire undoped polysilicon material layer has been consumed and made part of the grown oxide layer.

19. The method according to claim **17** wherein the step of forming a first polysilicon layer includes depositing doped polysilicon by low pressure chemical vapor deposition at a temperature in excess of 620 degrees centigrade, and further wherein the step of forming the second polysilicon layer includes depositing doped polysilicon by low pressure chemical vapor deposition at a temperature less than 600 degrees centigrade.

20. The method according to claim **17** which, prior to forming either of said first and second doped polysilicon layers, additionally comprises implanting dopant of a first polarity in adjacent regions of the semiconductor substrate, by a method comprising the steps of:

forming a first masking layer over said substrate which has a plurality of apertures therein,

providing a second mask over said first masking layer in a manner to cover a portion of said apertures from one side thereof, thereby leaving a first restricted opening to said substrate adjacent an opposite side of said apertures,

performing a first implant of impurities of a first polarity through said first restricted opening,

removing said second mask while maintaining said first masking layer in place,

forming a spacer within said apertures at least along said opposite side thereof, thereby forming a second restricted opening therethrough, and

providing a second implant of a second polarity opposite to said first polarity through said second restricted opening,

whereby said spacer protects the surface of said semiconductor substrate implanted with said impurities of the first polarity from overcompensation from said second implant of the opposite second polarity.

21. A method of forming a plurality of flash electrically erasable and programmable read only memory cells on a semiconductor substrate, comprising the steps of:

forming a first layer of doped polysilicon conductive material across two adjacent of said memory cells and insulated from said substrate by first dielectric layer,

forming a second dielectric layer over said first polysilicon layer,

forming a second layer of doped polysilicon conductive material as a control gate over each of said adjacent memory cells,

forming a third dielectric layer across said control gate and exposed portions of said second dielectric layer therebetween,

forming a mask over said third dielectric layer with an aperture therein positioned between the adjacent cells but over the first polysilicon layer extending therebetween,

removing the third dielectric layer under the aperture of said photoresist mask, thereby exposing said first polysilicon layer,

growing oxide through the mask aperture on the first polysilicon layer in a manner that the first polysilicon layer is completely consumed, thereby separating the first doped polysilicon layer into a separate floating gate for each of said at least two adjacent cells, and

forming an erase gate through said mask aperture.

22. A method of forming a layer of oxide on a doped polysilicon conductor that is an electrically isolated floating gate provided as part of an integrated circuit, including the steps of:

forming a layer of an undoped polysilicon material on said doped polysilicon surface,

thereafter growing a layer of oxide on the undoped polysilicon material layer for a time until substantially the entire undoped polysilicon material layer has been consumed and made part of the grown oxide layer, and

forming a conductive erase gate over at least a portion of said grown oxide layer.

23. A method of forming an array of memory cells on a semiconductor substrate, comprising:

forming a thin layer of gate oxide insulating material across said substrate,

forming a first set of substantially parallel strips of doped polysilicon material across said oxide in order to form a first set of elongated electrically conductive strips thereacross,

thereafter forming a layer of undoped polysilicon material extending over top surfaces of said gate oxide and said doped polysilicon material strips,

thereafter growing a layer of oxide on the undoped polysilicon material layer for a time until substantially the entire undoped polysilicon material layer has been consumed and made part of the grown oxide layer,

thereafter forming a second set of substantially parallel strips of doped polysilicon material across said layer of grown oxide in order to form a second set of elongated electrically conductive strips thereacross, said first and second sets of conductive strips having their lengths oriented substantially orthogonal to each other, and

thereafter removing portions of said first set of conductive strips between said second set of conduc-

tive strips, thereby forming a plurality of electrically isolated gates along the length of each of said first set of conductive strips.

24. A method of forming an electrically erasable and programmable read only memory having a doped polysilicon floating gate separate from a semiconductor substrate and from a doped polysilicon control gate by oxide insulating layers, and an erase gate separated from a portion of said floating gate by an erase oxide, comprising the steps of:

depositing said floating gate polysilicon layer in excess of 620° C.,

growing said erase gate oxide over a portion of the surface of said floating gate polysilicon layer,

depositing said control gate polysilicon layer by a temperature of less than 600° C.,

growing an insulating oxide layer over said control gate polysilicon layer, and

forming a conductive erase gate in a position to be separated from said floating gate by said erase gate oxide and from said control gate by said insulating oxide layer.

25. A method of implanting dopant of opposite conductivity type in adjacent regions of a semiconductor substrate, comprising the steps of:

forming a first masking layer over said substrate which has a plurality of apertures therein,

providing a second mask over said first masking layer in a manner to cover a portion of said apertures from one side thereof, thereby leaving a first restricted opening to said substrate adjacent an opposite side of said apertures,

performing a first implant of impurities of a first polarity through said first restricted opening,

removing said second mask while maintaining said first masking layer in place,

forming a spacer within said apertures at least along said opposite side thereof, thereby forming a second restricted opening therethrough, and

providing a second implant of a second polarity opposite to said first polarity through said second restricted opening,

whereby said spacer protects the surface of said semiconductor substrate implanted with impurities of the first polarity from overcompensation from said second implant of the opposite second polarity.

26. The method according to claim 25 which comprises an additional step of thereafter growing a layer of thick oxide in said substrate through said second restricted opening.

27. A method of forming an array of a plurality of memory cells on a semiconductor substrate, comprising the steps of:

forming a doped polysilicon strip extending across at least two adjacent memory cells and insulated from said substrate by a thin insulating layer therebetween,

protecting the polysilicon strip by a mask that leaves a portion thereof between said at least two cells exposed, and

oxidizing said exposed doped polysilicon until the exposed portion is completely consumed by the oxidation process, thereby leaving electrically separate floating gates associated with each of said adjacent cells.

28. The method according to claim 27 wherein said mask is provided, at least in part, by a patterned layer of doped polysilicon in each of said adjacent cells positioned over said polysilicon strip with an insulating layer therebetween.

29. The method according to claim 27 wherein said exposed polysilicon strip portion is defined by an aperture in a photoresist mask.

30. The method according to claim 1 which comprises the following additional steps performed after the electrically isolated floating gates have been formed:

reducing the size of the spacers in a manner to expand said gap, thereby exposing surface area portions of said floating gates adjacent said spacers,

forming a third dielectric layer over the exposed surface area of the floating gates, and

forming a third plurality of elongated strips of conductive material across said third dielectric layer within at least a portion of said expanded gap and in a manner to be substantially parallel with each other and with said second plurality of conductive strips, thereby forming erase gates.

* * * * *

EXHIBIT L

PACER Case Locator

Civil Party Search
Thu Sep 30 19:10:24 2010
99 records found

User: sa0307
Client: 084600-00014 dhsearch
Search: Civil Party Search Name STMicro NOS 830 All Courts Page: 1 sort: cs_date_filed

	Party Name	Court	Case	NOS	Date Filed ▼	Date Closed
1	STMicroelectronics, Inc. (cc)	azdce	2:1998-cv-01413	830	07/31/1998	07/16/2007
2	STMicroelectronics, Inc. (dft)	azdce	2:1998-cv-01413	830	07/31/1998	07/16/2007
3	Stmicroelectronics (RB) Inc (dft)	txedce	2:1999-cv-00168	830	08/27/1999	09/30/2002
4	Stmicroelectronics Inc (dft)	txedce	2:1999-cv-00168	830	08/27/1999	09/30/2002
5	Stmicroelectronics NV (condft)	txedce	2:1999-cv-00168	830	08/27/1999	09/30/2002
6	Stmicroelectronics SRL (dft)	txedce	2:1999-cv-00168	830	08/27/1999	09/30/2002
7	STMicroelectronics Inc (cd)	txndce	3:2000-cv-01573	830	07/21/2000	01/12/2001
8	STMicroelectronics Inc (pla)	txndce	3:2000-cv-01573	830	07/21/2000	01/12/2001
9	Stmicroelectronics, Inc. (cc)	dedce	1:2000-cv-00833	830	09/13/2000	01/02/2001
10	Stmicroelectronics, Inc. (dft)	dedce	1:2000-cv-00833	830	09/13/2000	01/02/2001
11	STMicroelectronics Inc (dft)	txndce	3:2000-mc-00080	830	09/14/2000	10/03/2001
12	Stmicroelectronics NV, . (dft)	txedce	2:2000-cv-00208	830	10/03/2000	03/30/2004
13	STMicroelectronics, Inc. (cc)	nysdce	1:2001-cv-05012	830	06/06/2001	02/19/2003
14	STMicroelectronics, Inc. (dft)	nysdce	1:2001-cv-05012	830	06/06/2001	02/19/2003
15	STMicroelectronics Inc (pla)	txndce	3:2001-cv-01079	830	06/06/2001	10/18/2001
16	Stmicroelectronics (RB) Inc. (dft)	nyedce	2:2002-cv-03475	830	06/14/2002	01/18/2005
17	Stmicroelectronics Inc. (cc)	nyedce	2:2002-cv-03475	830	06/14/2002	01/18/2005
18	Stmicroelectronics Inc. (dft)	nyedce	2:2002-cv-03475	830	06/14/2002	01/18/2005
19	Stmicroelectronics Inc (cd)	txedce	4:2002-cv-00362	830	11/07/2002	04/27/2004
20	Stmicroelectronics Inc (pla)	txedce	4:2002-cv-00362	830	11/07/2002	04/27/2004
21	Stmicroelectronics Inc (cc)	txedce	1:2003-cv-00407	830	07/01/2003	12/17/2004
22	Stmicroelectronics Inc (cd)	txedce	1:2003-cv-00407	830	07/01/2003	12/17/2004
23	Stmicroelectronics Inc (dft)	txedce	1:2003-cv-00407	830	07/01/2003	12/17/2004
24	STMicroelectronics NV (cc)	txedce	1:2003-cv-00407	830	07/01/2003	12/17/2004
25	STMicroelectronics NV (dft)	txedce	1:2003-cv-00407	830	07/01/2003	12/17/2004
26	STMicroelectronics Inc (cc)	txedce	4:2003-cv-00276	830	07/18/2003	12/27/2004
27	STMicroelectronics Inc (cd)	txedce	4:2003-cv-00276	830	07/18/2003	12/27/2004
28	STMicroelectronics Inc (pla)	txedce	4:2003-cv-00276	830	07/18/2003	12/27/2004
29	Stmicroelectronics NV (3pd)	txedce	4:2003-cv-00276	830	07/18/2003	12/27/2004
30	Stmicroelectronics NV (cc)	txedce	4:2003-cv-00276	830	07/18/2003	12/27/2004
31	Stmicroelectronics NV (cd)	txedce	4:2003-cv-00276	830	07/18/2003	12/27/2004
32	STMicroelectronics NV (cc)	candce	5:2004-cv-04379	830	10/15/2004	09/17/2009
33	STMicroelectronics NV (cd)	candce	5:2004-cv-04379	830	10/15/2004	09/17/2009
34	STMicroelectronics NV (dft)	candce	5:2004-cv-04379	830	10/15/2004	09/17/2009
35	STMicroelectronics, Inc. (cc)	candce	5:2004-cv-04379	830	10/15/2004	09/17/2009
36	STMicroelectronics, Inc. (cd)	candce	5:2004-cv-04379	830	10/15/2004	09/17/2009
37	STMicroelectronics, Inc. (dft)	candce	5:2004-cv-04379	830	10/15/2004	09/17/2009
38	STMicroelectronics Inc (pla)	txedce	4:2005-cv-00044	830	02/04/2005	02/06/2007
39	STMicroelectronics Inc (cc)	txedce	4:2005-cv-00045	830	02/04/2005	06/25/2007
40	STMicroelectronics Inc (cd)	txedce	4:2005-cv-00045	830	02/04/2005	06/25/2007
41	STMicroelectronics Inc (pla)	txedce	4:2005-cv-00045	830	02/04/2005	06/25/2007
42	STMicroelectronics N.V. (dft)	candce	5:2005-cv-01248	830	03/28/2005	04/11/2005
43	STMicroelectronics,Inc., (dft)	candce	5:2005-cv-01248	830	03/28/2005	04/11/2005
44	STMicroelectronics,S.r.1., (dft)	candce	5:2005-cv-01248	830	03/28/2005	04/11/2005
45	STMicroelectronics Inc (cc)	candce	4:2005-cv-04063	830	10/07/2005	
46	STMicroelectronics Inc (dft)	candce	4:2005-cv-04063	830	10/07/2005	
47	STMicroelectronics N.V. (cc)	candce	4:2005-cv-04063	830	10/07/2005	
48	STMicroelectronics N.V. (dft)	candce	4:2005-cv-04063	830	10/07/2005	
49	STMicroelectronics, Inc. (cd)	candce	5:2005-cv-04691	830	11/16/2005	08/26/2008
50	STMicroelectronics, Inc. (pla)	candce	5:2005-cv-04691	830	11/16/2005	08/26/2008
51	STMicroelectronics NV (dft)	candce	5:2005-cv-05021	830	12/06/2005	08/29/2008
52	STMicroelectronics, Inc. (dft)	candce	5:2005-cv-05021	830	12/06/2005	08/29/2008
53	STMicroelectronics NV (dft)	candce	5:2006-cv-00194	830	01/11/2006	05/17/2006
54	STMicroelectronics, Inc. (dft)	candce	5:2006-cv-00194	830	01/11/2006	05/17/2006

PACER Case Locator

Civil Party Search
Thu Sep 30 19:10:24 2010
99 records found

User: sa0307
Client: 084600-00014 dhsearch
Search: Civil Party Search Name STMicro NOS 830 All Courts Page: 2 sort: cs_date_filed

	Party Name	Court	Case	NOS	Date Filed ▼	Date Closed
55	STMicroelectronics Inc. (cc)	dedce	1:2006-cv-00627	830	10/10/2006	10/17/2008
56	STMicroelectronics Inc. (crd)	dedce	1:2006-cv-00627	830	10/10/2006	10/17/2008
57	Stmicroelectronics, Inc. (3pd)	dedce	1:2006-cv-00785	830	12/21/2006	
58	Stmicroelectronics, Inc. (cd)	dedce	1:2006-cv-00785	830	12/21/2006	
59	Stmicroelectronics, Inc. (dft)	dedce	1:2006-cv-00785	830	12/21/2006	
60	STMicroelectronics, Inc. (dft)	txedce	2:2007-cv-00278	830	07/02/2007	05/24/2010
61	Stmicroelectronics Inc (dft)	txedce	2:2007-cv-00515	830	11/27/2007	03/04/2008
62	STMicroelectronics NV (dft)	txedce	2:2008-cv-00165	830	04/21/2008	
63	STMicroelectronics, Inc. (pla)	candce	5:2008-cv-02332	830	05/06/2008	08/26/2008
64	STMicroelectronics Inc (cc)	txndce	3:2008-cv-00977	830	06/09/2008	
65	STMicroelectronics Inc (dft)	txndce	3:2008-cv-00977	830	06/09/2008	
66	STMicroelectronics NV (cc)	txndce	3:2008-cv-00977	830	06/09/2008	
67	STMicroelectronics NV (dft)	txndce	3:2008-cv-00977	830	06/09/2008	
68	Stmicroelectronics Inc (cc)	cacdce	8:2008-cv-01039	830	09/17/2008	07/15/2010
69	Stmicroelectronics Inc (dft)	cacdce	8:2008-cv-01039	830	09/17/2008	07/15/2010
70	Stmicroelectronics N V (cc)	cacdce	8:2008-cv-01039	830	09/17/2008	07/15/2010
71	Stmicroelectronics N V (dft)	cacdce	8:2008-cv-01039	830	09/17/2008	07/15/2010
72	STMicroelectronics, Inc. (3pd)	txndce	3:2008-cv-02075	830	11/20/2008	
73	Stmicroelectronics Corporation (dft)	candce	3:2009-cv-01244	830	03/23/2009	07/20/2010
74	STMicroelectronics N.V. (dft)	candce	3:2009-cv-01244	830	03/23/2009	07/20/2010
75	STMicroelectronics, Inc. (dft)	candce	3:2009-cv-01244	830	03/23/2009	07/20/2010
76	STMicroelectronics N.V. (dft)	gandce	1:2009-cv-01098	830	04/24/2009	07/09/2010
77	STMicroelectronics, Inc. (cc)	gandce	1:2009-cv-01098	830	04/24/2009	07/09/2010
78	STMicroelectronics, Inc. (dft)	gandce	1:2009-cv-01098	830	04/24/2009	07/09/2010
79	STMicroelectronics (dft)	candce	3:2009-cv-04243	830	09/14/2009	07/08/2010
80	STMicroelectronics, Inc. (dft)	madce	1:2009-cv-11933	830	11/11/2009	
81	STMicroelectronics (ip)	gandce	1:2009-cv-03391	830	12/03/2009	06/11/2010
82	Stmicroelectronics, Inc. (cc)	candce	3:2009-cv-05962	830	12/22/2009	08/24/2010
83	Stmicroelectronics, Inc. (dft)	candce	3:2009-cv-05962	830	12/22/2009	08/24/2010
84	STMicroelectronics Inc (dft)	txndce	3:2010-cv-00481	830	03/09/2010	03/18/2010
85	STMicroelectronics NV (dft)	txndce	3:2010-cv-00481	830	03/09/2010	03/18/2010
86	Stmicroelectronics, Inc. (dft)	dedce	1:2010-cv-00206	830	03/15/2010	
87	STMicroelectronics, N.V. (dft)	dedce	1:2010-cv-00206	830	03/15/2010	
88	STMicroelectronics, Inc. (cc)	txedce	2:2010-cv-00090	830	03/15/2010	
89	STMicroelectronics, Inc. (dft)	txedce	2:2010-cv-00090	830	03/15/2010	
90	STMicroelectronics, N.V. (cc)	txedce	2:2010-cv-00090	830	03/15/2010	
91	STMicroelectronics, N.V. (dft)	txedce	2:2010-cv-00090	830	03/15/2010	
92	STMicroelectronics, Inc. (cc)	txedce	6:2010-cv-00092	830	03/15/2010	
93	STMicroelectronics, Inc. (dft)	txedce	6:2010-cv-00092	830	03/15/2010	
94	STMicroelectronics, N.V. (dft)	txedce	6:2010-cv-00092	830	03/15/2010	
95	STMicroelectronics (ip)	cacdce	2:2010-cv-04370	830	06/14/2010	
96	STMicroelectronics, Inc. (dft)	txedce	2:2010-cv-00216	830	06/30/2010	
97	STMicroelectronics, N.V. (dft)	txedce	2:2010-cv-00216	830	06/30/2010	
98	STMicroelectronics Inc (cd)	txndce	3:2010-cv-01460	830	07/23/2010	
99	STMicroelectronics Inc (pla)	txndce	3:2010-cv-01460	830	07/23/2010	