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UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

Commissioners: **Timothy J. Muris, Chairman**
Sheila F. Anthony
Mozelle W. Thompson
Orson Swindle
Thomas B. Leary

In the Matter of	)	
RAMBUS INCORPORATED,	)	**DOCKET NO. 9302**
a corporation.	)	

COMPLAINT

Pursuant to the provisions of the Federal Trade Commission Act, and by virtue of the authority vested in it by said Act, the Federal Trade Commission ("Commission"), having reason to believe that Rambus Incorporated (hereinafter, "Rambus" or "Respondent") has violated Section 5 of the Federal Trade Commission ("FTC") Act, as amended, 15 U.S.C. § 45, and it appearing to the Commission that a proceeding in respect thereof would be in the public interest, hereby issues its complaint, stating its charges as follows:

Nature of the Case

1. Through this action, the Commission challenges a pattern of anticompetitive acts and practices, undertaken by Rambus over the course of the past decade, and continuing even today, whereby Rambus, through deliberate and intentional means, has illegally monopolized, attempted to monopolize, or otherwise engaged in unfair methods of competition in certain markets relating to technological features necessary for the design and manufacture of a common form of digital computer memory, known as dynamic random access memory, or "DRAM."

2. Rambus's anticompetitive scheme involved participating in the work of an industry standard-setting organization, known as JEDEC, without making it known to JEDEC or to its members that Rambus was actively working to develop, and did in fact possess, a patent and several pending patent applications that involved specific technologies proposed for and ultimately adopted in the relevant standards. By concealing this information – in violation of JEDEC's own operating rules and procedures – and through other bad-faith, deceptive conduct, Rambus purposefully sought to and did convey to JEDEC the materially false and misleading impression that it possessed no relevant intellectual property rights. Rambus's anticompetitive scheme further entailed perfecting its patent rights over these same technologies and then, once the standards had become widely adopted within the DRAM industry, enforcing such patents worldwide against companies manufacturing memory products in compliance with the standards.

3. The pattern of anticompetitive conduct by Rambus that is at issue in this action has materially caused or threatened to cause substantial harm to competition, and will in the future materially cause or threaten to cause further substantial injury to competition and to consumers, absent the issuance of appropriate relief in the manner set forth below.

The Respondent

4. Rambus is a public corporation organized, existing, and doing business under and by virtue of the laws of the State of Delaware, with its office and principal place of business located at 9440 El Camino Real, Los Altos, California 94022.

5. Rambus designs, develops, licenses, and markets high-speed chip-connection technology to enhance the performance of computers, consumer electronics, and communications systems. The company licenses semiconductor companies to manufacture and sell memory and logic integrated circuits incorporating Rambus chip-connection technology and markets its solutions to systems companies to encourage them to design this technology into their products. For the fiscal year that ended on September 30, 2001, Rambus reported revenues of approximately $117 million.

6. Rambus is, and at all relevant times has been, a corporation as "corporation" is defined by Section 4 of the Federal Trade Commission Act, 15 U.S.C. § 44; and at all times relevant herein, Rambus has been, and is now, engaged in commerce as "commerce" is defined in the same provision.

Background on the DRAM Industry

7. Within the array of components that together comprise a typical computer, the computer's "memory" functions to store digitally recorded information such that it is available to be

accessed when needed by the central processing unit ("CPU"). Computer memory is produced in the form of semiconductor "chips," which are connected with other computer components – such as the CPU and the chipset – via a collection of circuit lines, or a "bus," that routes electronic signals and, in this way, communicates commands and transports data.

8. DRAM is the most common form of computer memory in use today. Another form of memory is known as static random access memory, or "SRAM." DRAM and SRAM differ principally in the following ways: SRAM, unlike DRAM, is able to continuously hold information while power is being supplied to memory. With DRAM, on the other hand, the electronic charges that serve to hold the stored information in place dissipate over time, causing information to "leak" out of memory. To counteract this phenomenon, DRAM memory chips must be constantly "refreshed" with new electronic pulses. DRAM and SRAM also differ in that the latter generally is both faster and more expensive.

9. DRAM is an essential input into a variety of downstream products, including a wide variety of computers, such as personal computers, work stations, and servers, as well as various other types of electronic devices, such as fax machines, printers, digital video recorders, video game equipment, and personal digital assistants. Total sales of DRAM in the United States exceeded $12 billion in 2000, and for the same year worldwide DRAM sales exceeded $28 billion.

10. Over the years, a series of different architectures for designing DRAM chips has been introduced. As in most other aspects of the computer industry, over time older-generation designs have given way to newer-generation designs or to improvements on existing architectures. A driving force behind this continual process of evolution in DRAM design is the quest for improved computer performance. In particular, as the performance of other computer components and subsystems is enhanced, the marketplace demands equivalent improvements in the speed and other performance characteristics of computer memory.

11. During the late 1980s and early 1990s, developments and improvements in the performance of CPUs and other computer components were moving forward at a rapid clip. It was perceived, however, that developments in DRAM technology had not kept pace, and that performance constraints inherent in the available DRAM architectures were hindering technological progress in the computer industry, creating a virtual "memory bottleneck."

12. It was in this environment that "synchronous" DRAM was developed. The essential innovation underlying synchronous DRAM – as compared to the prior generation of DRAM, also known as "asynchronous" DRAM – was to link memory functions to a "system clock," allowing for more rapid sequencing of communications between the CPU and memory, thereby improving overall system performance. The system clock, in effect, consists of a continuous series of evenly spaced electronic pulses. The period of time (measured in nanoseconds) elapsing between the initiation of two succeeding pulses is referred to as a single "clock cycle."

13. The introduction of synchronous DRAM offered a potentially promising solution to the memory bottleneck. Yet the success of synchronous DRAM depended importantly upon the ability of the computer industry to adopt standards governing the design and implementation of synchronous DRAM.

JEDEC

14. The JEDEC Solid State Technology Association ("JEDEC") – originally known as the Joint Electron Device Engineering Council, from which the acronym JEDEC derives – is one of several standard-setting bodies affiliated with the Electronic Industries Alliance ("EIA"), a trade association representing all segments of the electronics industry. As explained in JEDEC's Manual of Organization and Procedure (hereinafter, the "JEDEC Manual"), the organization's primary purpose and function is to "promote the development and standardization of terms, definitions, product characterization, test methods, manufacturing support functions and mechanical standards for solid state products."

15. According to the JEDEC Manual, membership in JEDEC is freely available to "[a]ny company, organization, or individual conducting business in the USA that … manufactures electronic equipment or electronics-related products, or provides electronics or electronics-related services." To become a JEDEC member, an eligible company need only submit an application, pay membership fees, and agree to abide by JEDEC's rules. JEDEC members, currently numbering in excess of 200, include many of the world's top designers and manufacturers of semiconductors and related products, as well as many of the largest purchasers of such products.

16. JEDEC's internal structure consists of a Board of Directors (formerly known as the JEDEC "Council") and numerous operational committees, subcommittees, and task groups. Standards typically are proposed, evaluated, and formalized at the committee or subcommittee level and then presented for approval to the Board of Directors, which has final authority to approve or disapprove all proposed standards.

JEDEC Policies and Procedures

17. At all times relevant herein, JEDEC has steadfastly maintained a commitment to promoting free competition within the semiconductor industry. Thus, JEDEC has insisted that its members abide by all applicable laws, including but not limited to laws prohibiting anticompetitive conduct.

18. The JEDEC Manual provides that all JEDEC meetings "shall comply with the current edition of EIA Legal Guides." These Legal Guides – which are explicitly "incorporated … by reference" into JEDEC's own governing rules, and currently are posted on JEDEC's own website under the heading "Manuals" – provide that standardization programs must be "conducted under strict policies designed to promote and stimulate our free enterprise system and to make sure that laws for maintaining and preserving this system are vigorously followed."

19. The EIA/JEDEC Legal Guides establish a "basic rule" that standardization programs conducted by the organization "shall not be proposed for or indirectly result in … restricting competition, giving a competitive advantage to any manufacturer, [or] excluding competitors from the market."

20. Consistent with its commitment to promoting unfettered competition, at all times relevant herein JEDEC also has maintained a commitment to avoid, where possible, the incorporation of patented technologies into its published standards, or at a minimum to ensure that such technologies, if incorporated, will be available to be licensed on royalty-free or otherwise reasonable and non-discriminatory terms. Toward this end, JEDEC has implemented procedures designed to ensure that members disclose any patents, or pending patent applications, involving the standard-setting work being undertaken by the organization.

21. At all times relevant herein, meetings of the pertinent JEDEC subcommittee routinely were opened with a statement by the chairperson underscoring the existence of such disclosure obligations. This practice is in conformity with requirements set forth in the JEDEC Manual, the current edition of which provides:

> "The chairperson of any JEDEC committee [expressly defined to include, among other things, subcommittees] must call to the attention of all those present the requirements contained in EIA Legal Guides, and the obligation of all participants to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking."

Although the above provision was first added to the JEDEC Manual in October 1993, the existence and scope of these disclosure obligations were commonly known within JEDEC before that time, and indeed throughout the entirety of Rambus's involvement in the organization, from late 1991 through mid-1996.

22. While JEDEC does not altogether prohibit the use of patented items in the standards that it promulgates, the JEDEC Manual does mandate that the use of such items "be considered with great care." Indeed, consistent with procedures and practices followed within JEDEC throughout the relevant time period, the JEDEC Manual, at least since October 1993, has

required that no standard be drafted to include "patented items" – or "items and processes for which a patent has been applied" – absent both

(1) a well-supported technical justification for inclusion of the patented item; and

(2) express written assurance from the patent holder that a license to the patented technology will be made available either "without compensation" or under "reasonable terms and conditions that are demonstrably free of any unfair discrimination."

23. The JEDEC Manual, at least since October 1993, has expressly provided that the disclosure and licensing obligations discussed above apply "with equal force" when JEDEC members, subsequent to the adoption of a standard, discover new information about existing patent rights – or otherwise obtain new patent rights – involving that standard. In such situations, the JEDEC member must make the same disclosures and provide the same assurances as would be required if the member knew of such patent rights prior to adoption of the relevant standard.

24. Fairly interpreted, the policies, procedures, and practices existing within JEDEC throughout all times relevant herein imposed upon JEDEC members certain basic duties with regard to the disclosure of relevant patent-related information and the licensing of relevant patent rights:

a. First, to the extent any JEDEC member knew or believed that it possessed patents or pending patent applications that might involve the standard-setting work that JEDEC was undertaking, the member was required to disclose the existence of the relevant patents or patent applications and to identify the aspect of JEDEC's work to which they related.

b. Second, in the event that technologies covered by a member's known patents or patent applications were proposed for inclusion in a JEDEC standard, the member was required to state whether the technology would be made available either "without compensation" or under "reasonable terms and conditions that are demonstrably free of any unfair discrimination." Absent the member's agreement to one of these two conditions, the JEDEC rules would not allow the technology to be incorporated into a proposed standard.

JEDEC Work Involving SDRAM Standards

25. The JEDEC committee responsible for overseeing the development of standards relating to memory devices is known as the JC-42 Committee on Solid State Memories ("JC-42"), which has several subcommittees, one of which is particularly relevant for purposes of the instant

complaint: the JC-42.3 Subcommittee on RAM Devices ("JC-42.3").

26. Beginning in or around 1990, JC-42.3 commenced work on standards relating to the design and architecture of synchronous DRAM, referred to within JC-42.3 as "SDRAM." JEDEC members involved in the SDRAM-related work of JC-42.3 have over time included virtually all leading memory designers, manufacturers, and users, whether based in the U.S. or abroad.

27. During the 1990s, JEDEC issued several SDRAM-related standards, the first of which was published in November 1993 and was identified as Release 4 of the 21-C Standard. Subsequent releases of the 21-C Standard followed after that, only small portions of which related to SDRAM, as opposed to other memory-related technologies. In August 1999, however, JEDEC published a substantially augmented SDRAM standard – Release 9 of the 21-C Standard – which introduced a second generation of SDRAM. This second-generation standard became known as "double data rate," or "DDR," SDRAM.

28. Although the second-generation SDRAM standard was not issued until 1999, the work that culminated in that standard commenced, at the very latest, shortly after the first-generation SDRAM standard was adopted in 1993. Indeed, it may have commenced even earlier than that, inasmuch as at least one of the technological features initially considered (but ultimately rejected) for the first-generation SDRAM standard was later adopted in the second-generation standard. In addition, most, if not all, of the technologies encompassed in the first SDRAM standard were carried forward in the second-generation standard as well.

29. The process through which JEDEC adopted and published these standards proceeded essentially as follows:

    a. At regularly scheduled meetings of the JC-42.3 Subcommittee, which typically occurred on a quarterly basis – as well as affiliated committee and task group meetings, which were scheduled as needed – members were allowed to make presentations concerning specific concepts or technologies they proposed for inclusion in a standard under development.

    b. Such presentations generally were accompanied by written materials, which, in addition to being shared with all members present at the meeting, were reproduced and attached to the official meeting minutes.

    c. Before any proposal could be considered for adoption, it was necessary that it be presented a second time at a later subcommittee meeting.

    d. At that point, a member could move that the proposal be presented to the

subcommittee membership for approval through a formal balloting process, pursuant to which written ballots were distributed and received by mail.

e. Votes were then tabulated at the subsequent meeting of the subcommittee, at which time members voting "No" were required to explain their reasons for opposing the proposal.

f. Technically, a two-thirds majority was required, but in practice proposals rarely passed without a consensus of all voting members.

g. Individual proposals, once approved by JC-42.3, were often held at the subcommittee level until a complete package of related proposals was ready to be forwarded to the Council for final ratification.

30. JEDEC's – specifically, the JC-42.3 Subcommittee's – work on SDRAM standards continues today, and a third-generation SDRAM standard, known as "DDR II," is expected to be completed later this year.

Rambus and Its Proprietary RDRAM Technology

31. Rambus was founded in 1990 by two electrical engineers, Mark Horowitz and Michael Farmwald, who together developed their own, proprietary synchronous DRAM architecture. They named the new architecture Rambus DRAM, or simply "RDRAM," and contributed the technology to the new corporation upon its formation.

32. RDRAM, as originally designed, differed from traditional DRAM architectures in several ways, including but not limited to the following:

a. First, the RDRAM architecture specified the use of many fewer bus lines than was common in traditional DRAM designs. Thus, RDRAM was said to be a "narrow-bus" architecture. By comparison to RDRAM, traditional DRAM incorporated what was referred to as a "wide-bus" or "broad-bus" design.

b. Second, in the RDRAM architecture, each bus line was capable of carrying three types of information essential to memory functionality: (1) data; (2) "address" information, specifying the location where needed data could be found, or should be placed, in memory; and (3) "control" information, specifying, among other things, the relevant command (*e.g.*, whether the computer should "read" data from memory or "write" new data to memory). By comparison, in traditional DRAM architectures, each bus line was generally dedicated to carrying only one of these three types of information. Thus,

the RDRAM bus was sometimes said to be "multiplexed" or "triply multiplexed."

c. Third, rather than transmitting data, address, and control information separately, as was common in a traditional DRAM architecture, RDRAM transmitted such information together in groupings, called "packets." For this reason, RDRAM is also sometimes referred to as a "packetized" system.

33. Though Rambus has designed, and obtained patents on, various DRAM-related technological concepts or features, Rambus does not itself manufacture such technologies, choosing instead to license its designs for a fee to downstream memory manufacturers. Beginning in the early 1990s and continuing through the present, Rambus has sought to market and license its proprietary RDRAM technology to manufacturers of computer memory and related products, including a number of companies holding membership in JEDEC.

Rambus's '898 Patent Application and Its Progeny

34. On April 18, 1990, Rambus filed its first DRAM-related patent application with the United States Patent and Trademark Office ("PTO") – Application No. 07/510,898 (hereinafter, "the '898 application"). The application contained a 62-page specification and 15 drawings, all purporting to describe Rambus's DRAM-related inventions. In addition, the '898 application contained 150 separate claims, each of which was limited to a narrow-bus, multiplexed, packetized DRAM design.

35. Patents and patent applications consist of two principal parts. The first part is a written description, whereby the patent applicant (or, if the application issues as a patent, the patent holder) describes the invention, through technical specifications and drawings, in a manner that would allow a person skilled in the art to which the invention applies to understand and practice the invention without undue experimentation. The second part of the patent or patent application consists of one or more "claims" defining, or delineating, the scope – or outer bounds – of the patent holder's exclusive rights (or, in the case of an application, the exclusive rights the applicant seeks to obtain).

36. Because all 150 claims contained in Rambus's '898 patent application were limited to a narrow-bus, multiplexed, packetized DRAM design, through this application Rambus was not seeking – nor, absent amendment to the application, could it obtain – any patent rights exceeding those limitations.

37. In March 1992, Rambus broke out portions of its '898 application into 10 divisional patent applications, each of which "claimed priority back" to the '898 application and to its April 1990 filing date. The original '898 application and these 10 divisional applications, in turn, gave rise

to numerous other amended, divisional, or continuation patent applications – all technically the "progeny" of the '898 application – and eventually resulted in the issuance of numerous Rambus patents.

a. The process of obtaining patents or "perfecting" patent claims, otherwise known as patent prosecution, often involves amending, dividing, or continuing patent applications on file with the PTO.

b. Through an "amendment" to a pending patent application, a patent applicant may delete or alter certain claims contained in the pending application, or may add new claims, while at the same time retaining the same specification, drawings, and (to the extent not amended or deleted) claims of the previously pending application.

c. A "divisional" application is one that carves out one of multiple distinct inventions from a prior application and seeks to obtain patent rights over that distinct invention, without adding any new matter to the written description of the invention described in the earlier application.

d. A "continuation" application is a second application, covering the same invention described in a prior application, that is filed before the earlier application either issues as a patent or is abandoned and, again, adds no new matter to the written description of the invention described in the earlier application.

e. Before issuing any patent, the PTO first seeks to determine whether the invention claimed in the relevant patent application is preceded by "prior art" – that is, by preexisting inventions or other publicly known facts or information that demonstrates the lack of novelty in the invention for which a patent is sought.

f. Generally speaking, determinations of whether prior art exists in a given case are made by reference to the date on which the patent application is filed, otherwise known as the "priority date."

g. When a patent application is amended, divided, or continued in the manner described above, the patent applicant may "claim priority back" to an earlier-filed application – thus benefitting from the earlier filing date – but only if the amended, divisional, or continuation application "adds no new matter" to the written description of the invention described in the earlier application. As noted above, divisional and continuation applications, by definition, include no new matter not contained within the earlier-referenced application.

h. Subsequent amendments, divisionals, or continuations claiming priority back to an

earlier-filed patent application are sometimes said to be within the same "family" as the earlier-filed application, or otherwise are said to be the prior application's "progeny."

i. Thus, the fact that, as stated above, each Rambus patent application in the '898 "family" – or each of the '898 application's "progeny" – claimed priority back to the '898 application, means that all of the patent applications in the '898 family contained the same specification and drawings as were contained in the '898 application itself. In fact, in each amended, divisional, and continuation patent application Rambus filed claiming priority back to the '898 application's April 1990 filing date, Rambus was required to – and did – expressly warrant to the PTO that the application added "no new matter" beyond what was contained in the '898 application's 62-page specification and 15 drawings.

38. Though all of the Rambus patent applications in the '898 family contained the same specification and drawings as the '898 application itself, over time Rambus sought to expand the claims contained within these applications in order to obtain patent rights extending beyond the narrow-bus, multiplexed, packetized design inherent in the RDRAM design. In other words, in the course of prosecuting the '898 family of patent applications, Rambus made a conscious effort to withdraw the narrow-bus limitations contained in the original application's claims, and thereby sought to significantly expand the scope of its potential patent rights, while still clinging to the '898 application's April 1990 priority date.

Rambus's Initial Involvement in JEDEC

39. Even before Rambus was formally incorporated in early 1990, its founders outlined a strategy whereby, in an effort to obtain high royalties for RDRAM, they would seek to establish RDRAM as the actual or *de facto* industry standard.

40. Partly with this goal in mind, Rambus attended its first JEDEC meeting in December 1991, and it officially joined the organization shortly thereafter. Although JEDEC was conducting other potentially relevant work at that time, of particular relevance to Rambus was the work then underway within the JC-42.3 Subcommittee, which was in the process of developing a first generation of standards for SDRAM. From December 1991 through December 1995, Rambus representatives regularly attended JC-42.3 meetings.

41. Though Rambus attended its last JC-42.3 meeting in December 1995, it remained a member of JEDEC, and continued to receive official mailings and other information from JEDEC, until June 1996, when it formally withdrew from the organization.

Rambus's Scheme to Capture the SDRAM Standards

42. Shortly after becoming involved in JEDEC, it became apparent to Rambus that JC-42.3 was committed to developing SDRAM standards based on the traditional wide-bus, non-packetized DRAM architecture, relying to the extent possible on non-proprietary technologies. In other words, it was highly unlikely JC-42.3 would be interested in standardizing RDRAM, an architecture that was both proprietary and distinctly non-traditional.

43. Rambus, of course, would have preferred that its own RDRAM technology be adopted as the industry standard. Failing that, Rambus might have preferred to see any efforts at adopting an industry-wide SDRAM standard fail, inasmuch as industry adoption of such a standard would make it more difficult for Rambus to market its proprietary RDRAM technology. By mid-1992, however, Rambus had seized upon an alternative business plan – one that, if successful, might allow Rambus to achieve the goal of charging high royalties even if the DRAM industry were to adopt as its standard something other than RDRAM. Rambus's CEO, Geoff Tate, laid out this scheme in a June 18, 1992 draft of the Rambus 1992-1997 Business Plan:

> "For about 2+ years a JEDEC committee has been working on the specifications for a Synchronous DRAM. No standard has yet been approved by JEDEC. Our expectation is a standard will not be reached until end of 1992 at the earliest.
>
> * * *
>
> [W]e believe that Sync DRAMs infringe on some claims in our filed patents; and that there are additional claims we can file for our patents that cover features of Sync DRAMs. Then we will be in position to request patent licensing (fees and royalties) from any manufacturer of Sync DRAMs. Our action plan is to determine the exact claims and file the additional claims by the end of Q3/92. Then to advise Sync DRAM manufacturers in Q4/92."

44. In what appears to be the final draft of the same Rambus Business Plan, dated September 1992, Tate further elaborated on the scheme:

> "Rambus expects the patents will be issued largely as filed and that companies will not be able to develop Rambus-compatible or Rambus-like technology without infringing on multiple fundamental claims of the patents …. Rambus' patents are likely to have significant applications other than for the Rambus Interface."

In the same document, Tate also wrote: "Sync DRAMs infringe claims in Rambus's filed patents and other claims that Rambus will file in updates later in 1992."

45. In actuality, events unfolded somewhat differently than Rambus's CEO envisioned in these

statements, in a manner that affected the timing, but not the core substance, of Rambus's scheme. For instance, although Rambus's '898 application was pending at the time these statements were written, not until 1996 was Rambus – through a separate application claiming priority back to the '898 application – able to obtain its first patent broad enough to arguably cover aspects of the wide-bus DRAM architecture incorporated into the JEDEC standards. In addition, Rambus ultimately elected to wait until late 1999, after DRAM manufacturers and their customers had become "locked in" to the JEDEC standards, before seeking to enforce its patents against memory manufacturers producing JEDEC-compliant SDRAM.

46. Aside from such timing issues, the Rambus business plans quoted in Paragraphs 43 and 44 set forth quite accurately the basic scheme upon which the company would embark – that is, a scheme whereby Rambus would actively seek to perfect patent rights covering technologies that were the subject of an ongoing, industry-wide standardization process, in which Rambus itself was a regular participant, without disclosing the existence of such patent rights (or the pertinent patent applications) to other participants, many of whom, by producing products compliant with the standards, would later be charged with infringing Rambus's patents.

Implementation of Rambus's Scheme

47. During the course of its participation in JEDEC, from late 1991 through mid-1996, Rambus observed multiple presentations regarding technologies, proposed for (and later included in) JEDEC's SDRAM standards, that Rambus either (1) knew or believed to be covered by claims contained in its then-pending patent applications, or (2) believed could be covered through amendments to those applications expanding the scope of the patent claims while adding no new matter to the underlying technical specification.

48. That is, at all times relevant herein, Rambus believed that a number of the specific technologies that were proposed for, and later incorporated in, the relevant JEDEC standards were encompassed by the 62-page technical specification and 15 related drawings common to Rambus's '898 application (filed in 1990) and the numerous amended, divisional, and continuation applications that stemmed from the '898 application. Rambus further believed that, to the extent the pending claims of the '898 application and its later-filed progeny failed to cover these technologies as proposed to be used in JEDEC's SDRAM standards, such claims could be amended to cover these technologies, while still claiming priority back to the '898 application's April 1990 filing date.

49. As Rambus's CEO described in the company's internal planning documents in mid-1992 (*see* Paragraphs 43-44 above), the initial phase of Rambus's "action plan" required that it first "determine the exact claims" in its pending applications that covered technologies being incorporated into the JEDEC standards, and then, as needed, "file … additional claims" to

perfect Rambus's patent rights over such technologies. In executing these steps, Rambus placed heavy reliance upon two individuals: Richard Crisp, Rambus's designated representative to the JC-42.3 Subcommittee, and Lester Vincent, an attorney with the law firm of Blakely, Sokoloff, Taylor & Zafman, who served as Rambus's outside patent counsel.

50. Richard Crisp, an electrical engineer, joined Rambus in 1991. He attended his first JC-42.3 meeting in February 1992 and continued to attend such meetings regularly through December 1995. (In addition to Crisp, David Mooring, at that time Rambus's vice president for business development, and Billy Garrett, another Rambus engineer, sometimes attended JC-42.3 meetings.) In May 1992, Crisp became Rambus's designated representative to JC-42.3. As such, he personally received any information, such as meeting minutes and ballot forms, that JEDEC furnished to Rambus by mail.

51. Throughout the duration of Crisp's participation in the JC-42.3 Subcommittee, it was his customary practice to send comprehensive reports to his superiors and others within Rambus describing in detail the technologies that were being proposed for inclusion in the JEDEC SDRAM standards. Typically, these reports were communicated via e-mails authored and sent while the JC-42.3 meetings were still in progress.

52. Lester Vincent and his law firm, Blakely, Sokoloff, were retained as patent counsel by Rambus in the summer of 1991, at which time Vincent assumed primary responsibility for prosecuting Rambus's '898 application before the PTO. For several years thereafter, Vincent and his colleagues assisted Rambus with its DRAM-related patent strategy, providing frequent advice to Rambus on patent-related issues and assuming primary responsibility for drafting, filing, and prosecuting the various continuation and divisional patent applications that stemmed from the '898 application.

53. In late March 1992, Vincent met with Crisp and Allen Roberts, the Rambus vice president with responsibility for patents, to discuss, among other things, Rambus's participation in JEDEC. At this meeting, Vincent, Crisp, and Roberts discussed whether Rambus, having joined JEDEC and participated in JEDEC meetings, was at risk of forfeiting – on grounds of equitable estoppel – its rights to enforce future patents covering aspects of the JEDEC standards. Vincent advised that there could be an equitable estoppel problem if Rambus were to convey to other JEDEC participants the false or misleading impression that it would not seek to enforce its patents or its future patents. He further advised that, in order to reduce such risks, Rambus might remain silent and abstain from voting on any proposed JEDEC standards. Rambus in fact did abstain from voting on the scores of JC-42.3 ballot initiatives that arose during the course of its participation in JEDEC. Richard Crisp did vote on one occasion, however, registering a "No" vote on four separate ballot items.

54. Throughout its four and one-half years of participation in the JC-42.3 Subcommittee, Rambus engaged in a continuous pattern of deceptive, bad-faith conduct. Rambus's bad-faith participation in JEDEC, although evidenced in other ways as well, was perhaps best exemplified in the coordinated activities of Crisp and Vincent. During his four-year tenure as Rambus's representative to JC-42.3, Crisp observed multiple presentations relating to technologies Rambus believed were covered – or, through amendment, could be covered – by pending Rambus patent applications. In fact, in a number of instances, Crisp, while participating in JC-42.3 meetings, sent e-mails back to Rambus headquarters expressing a belief that Rambus had pending applications covering certain technologies being discussed in such meetings, or otherwise suggesting that Rambus's pending patent applications be reviewed, and if necessary amended, to ensure they covered such technologies. On several occasions, Crisp – based in part on information learned through attending JC-42.3 meetings – developed specific proposals for amending Rambus's pending patent claims and communicated such proposals directly (or via a Rambus colleague) to Vincent. Likewise, in some cases, Vincent sent copies of draft amendments to Rambus's patent applications to Crisp, among others, soliciting his input before finalizing such amendments. Plainly, in light of Rambus's failures to disclose pertinent patent-related information to JEDEC, the activities described in this paragraph constituted bad faith.

55. As underscored elsewhere in this complaint, Rambus never disclosed to JEDEC the fact that, throughout the duration of its membership in the organization, Rambus had on file with the PTO, and was actively prosecuting, patent applications that, in its view, either covered or could easily be amended to cover elements of the existing and future SDRAM standards.

Technologies Impacted by Rambus's Scheme

56. Among other specific technologies adopted or proposed for inclusion in the SDRAM standards during the period of Rambus's participation in JEDEC, which Rambus believed were covered by its then-pending patent applications or could be covered through amendments to such applications, were the following: (1) programmable CAS latency; (2) programmable burst length; (3) on-chip PLL/DLL; and (4) dual-edge clock.

57. Column address strobe (or "CAS") latency refers to the amount of time it takes for the memory to release data after receiving a signal, known as the column address strobe, in connection with a read request from the CPU. The technology known as programmable CAS latency allows memory chips to be programmed such that this aspect of the memory's operation can be tailored to facilitate compatibility with a variety of different computer environments.

58. Burst length generally refers to the number of times information (or data) is transmitted between the CPU and memory in conjunction with a single request or instruction. The technology

known as programmable burst length allows memory chips to be programmed to adjust this aspect of the memory's operation in order to facilitate compatibility with a variety of different computer environments.

59. From December 1991 through May 1992, Crisp and other Rambus representatives observed multiple JC-42.3 presentations pertaining to programmable CAS latency and programmable burst length, both of which were proposed to be incorporated in the first JEDEC SDRAM standard. Soon thereafter, in the summer of 1992, Crisp received, and voted upon, a ballot calling for inclusion of both technologies in the standard. This was the only time that Crisp voted on a JEDEC ballot, and he voted "No," for technical reasons that he was called upon to, and did, explain, but without saying anything to suggest that Rambus might possess relevant intellectual property.

60. At the time of these events, Crisp and others within Rambus believed that both programmable CAS latency and programmable burst length were encompassed by the inventions set forth in the specification and drawings of the '898 application and related applications that were then pending at the PTO, and that Rambus – by amending the claims in those pending applications – had the ability to perfect patent rights covering such technologies as used in the SDRAM standard. Indeed, beginning in May 1992, Crisp, Roberts, and other Rambus representatives began a series of consultations with Vincent for the purpose of drafting new claims, linked to the '898 application, that would cover use of certain technologies in the wide-bus architecture adopted by the SDRAM standard. Programmable CAS latency and programmable burst length were both among the technologies discussed for inclusion in these new wide-bus claims.

61. In March 1993, a Rambus representative attended the JC-42.3 meeting at which both programmable CAS latency and programmable burst length were approved for inclusion in the first SDRAM standard and were forwarded to the JEDEC Council, along with a collection of other approved technologies, as part of a comprehensive standard proposal. Despite Rambus's belief that these technologies were subject to pending Rambus patent claims, the Rambus representative remained silent throughout the meeting. In May 1993, the Council formally adopted the proposed SDRAM standard, which was published in November of that year. (Both of these technologies were later carried forward in the second-generation SDRAM standard published in August 1999.) Also in May 1993, Vincent's law firm (Blakely, Sokoloff) first filed patent claims on behalf of Rambus intended to cover use of DRAM technologies in a wide-bus architecture. From that time through the present, Rambus has continued its efforts to perfect patent rights covering use of programmable CAS latency and programmable burst length as incorporated in the SDRAM standards.

62. The design objectives served by inclusion of programmable CAS latency and programmable burst length technologies in the first- and second-generation JEDEC standards likely could have

been accomplished through use of alternative DRAM-related technologies available at the time these standards were developed. At a minimum, there would have been uncertainty at that time regarding the potential to identify or develop feasible alternative technologies. In either event, had Rambus disclosed to the JC-42.3 Subcommittee that it possessed pending patent applications purporting to cover – or that could be amended to cover – programmable CAS latency and burst length technologies in a wide-bus synchronous DRAM architecture, such disclosures likely would have impacted the content of the SDRAM standards, the terms on which Rambus would later be able to license any pertinent patent rights, or both.

63. Phase lock loop ("PLL") and delay lock loop ("DLL") are closely related technologies, both of which are used to synchronize the internal clock that governs operations within a memory chip and the system clock that regulates the timing of other system functions. The former, PLL, synchronizes the two clocks by adjusting the internal clock's frequency to match the system clock's frequency, whereas the latter, DLL, achieves synchronization by delaying the internal clock. "On-chip" PLL/DLL refers to the approach of placing these technologies on the memory chip itself, as opposed to the alternative approach of placing these technologies on, for instance, the memory module or the motherboard – the latter being known as "off-chip" PLL/DLL.

64. Beginning in September 1994, Crisp observed presentations and other work in the JC-42.3 Subcommittee involving proposals to include on-chip PLL in the second generation of the SDRAM standard. At that time, Crisp and others within Rambus believed that on-chip PLL was encompassed by the inventions set forth in the specification and drawings of the '898 application and related applications then pending at the PTO, and they had already discussed with Vincent their desire to perfect patent rights covering use of this technology in SDRAMs. Indeed, in June of 1993 Vincent's law firm filed, on Rambus's behalf, an amendment to a pending patent application – Application No. 07/847,692 – adding claims that, on their face, covered use of on-chip PLL/DLL technology in either a wide-bus or narrow-bus DRAM architecture. From June 1993 through the present, Rambus has continued its efforts to perfect patent rights covering use of on-chip DLL technology as ultimately incorporated in the second-generation SDRAM standard published in August 1999.

65. The design objectives served by inclusion of on-chip DLL technology in the second-generation JEDEC standard likely could have been accomplished through use of alternative DRAM-related technologies available at the time these standards were developed. At a minimum, there would have been uncertainty at that time regarding the potential to identify or develop feasible alternative technologies. In either event, had Rambus disclosed to the JC-42.3 Subcommittee that it possessed pending patent applications purportedly covering – or that could be amended to cover – on-chip PLL/DLL technologies in a wide-bus synchronous DRAM architecture,

such disclosures likely would have impacted the content of the SDRAM standards, the terms on which Rambus would later be able to license any pertinent patent rights, or both.

66. Dual-edge clock is a technology that permits information to be transmitted between the CPU and memory twice with every cycle of the system clock, thereby doubling the rate at which information is transmitted compared to the first generation of SDRAM, which incorporated a "single-edge clock" and hence permitted information to be transmitted only once per clock cycle.

67. Between December 1991 and April 1992, Crisp and other Rambus representatives attended JC-42.3 meetings at which they observed presentations and other work involving dual-edge clock technology and a closely related technology known as "toggle-mode." Ultimately, the JC-42.3 Subcommittee decided not to incorporate these technologies into the first-generation SDRAM standard. At the time this decision was reached, however, certain JC-42.3 members expressed the view that such technologies would be appropriate for reconsideration in connection with the next generation of SDRAM. Dual-edge clock technology was again discussed by the JC-42.3 Subcommittee in May 1995. Soon thereafter, in October 1995, a survey ballot relating in part to dual-edge clock technology was distributed to JC-42.3 members, and the same ballot was later discussed at a JC-42.3 meeting in December 1995. A formal proposal to include dual-edge clock technology in the second-generation SDRAM standard was made at a JC-42.3 Subcommittee meeting in March 1996. Following Rambus's withdrawal from JEDEC in June 1996, dual-edge clock technology was the subject of further presentations, and the technology ultimately was incorporated into the second-generation SDRAM standard.

68. In September 1994, Vincent's law firm, on behalf of Rambus, filed an amendment to Rambus's Patent Application No. 08/222,646, adding dual-edge clock claims that were not limited to a narrow-bus RDRAM design, but rather purported to cover use of dual-edge clock technology in any synchronous DRAM architecture, including a wide-bus architecture of the sort that was the focus of JEDEC's SDRAM standards. This application, as amended to include dual-edge clock claims, issued as U.S. Patent No. 5,513,327 (hereinafter, "the '327 patent") in April 1996, while Rambus was still a member of JEDEC. From September 1994 through the present, Rambus has continued its efforts to perfect patent rights covering use of dual-edge clock technology as used in a wide-bus synchronous DRAM architecture.

69. The design objectives served by inclusion of dual-edge clock technology in the second-generation SDRAM standard likely could have been accomplished through use of alternative DRAM-related technologies available at the time these standards were developed. At a minimum, there would have been uncertainty at that time regarding the potential to identify or develop feasible alternative technologies. In either event, had Rambus disclosed to the JC-42.3

Subcommittee that it possessed patents or pending patent applications arguably covering (or that, with respect the applications, could be amended to cover) dual-edge clock technology in a wide-bus synchronous DRAM architecture, such disclosures likely would have impacted the content of the SDRAM standards, the terms on which Rambus would later be able to license any pertinent patent rights, or both.

Rambus's Limited and Misleading Disclosures to JEDEC

70. At no time during its involvement in JEDEC did Rambus ever disclose to the organization the fact that it possessed an issued patent – the '327 patent discussed in Paragraph 68 above – that purported to cover use of a specific technology proposed for inclusion in the JEDEC SDRAM standards. Nor did Rambus ever disclose to JEDEC that it had on file with the PTO various pending patent applications that purported to cover, or could be amended to cover, a number of other technologies included or proposed for inclusion in the JEDEC SDRAM standards. More generally, Rambus never said or did anything to alert JEDEC to (1) Rambus's belief that it could claim rights to certain technological features not only when used in the context of its proprietary, narrow-bus, RDRAM designs, but also when used in the traditional wide-bus architecture that was the focus of JEDEC's SDRAM standard-setting activities; or (2) the fact that Rambus, while a member of JEDEC, was actively working to perfect such patent rights.

71. On the contrary, Rambus's very participation in JEDEC, coupled with its failure to make required patent-related disclosures, conveyed a materially false and misleading impression – namely, that JEDEC, by incorporating into its SDRAM standards technologies openly discussed and considered during Rambus's tenure in the organization, was not at risk of adopting standards that Rambus could later claim to infringe upon its patents.

72. On at least two occasions during Rambus's involvement in JEDEC, Crisp was asked by JEDEC representatives whether Rambus had any patent-related disclosures to make pertaining to technologies discussed within JC-42.3. In neither instance did Rambus elect to make such disclosures. One of these instances, however, prompted Rambus to present a letter to the JC-42.3 Subcommittee, dated September 11, 1995, which stated in part:

> "At this time, Rambus elects to not make a specific comment on our intellectual property position …. Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property."

73. Beyond these statements, the September 1995 letter said nothing concerning Rambus's patent position. In particular, it made no reference to the fact that Rambus possessed pending patent

applications that purported to cover, or were being amended to cover, both (1) technologies included in already published JEDEC standards, and (2) additional technologies then being considered for inclusion in future JEDEC standards. Moreover, the episode that gave rise to Rambus's September 1995 letter involved discussion of a narrow-bus, multiplexed, packetized SDRAM design – known as "SyncLink" – that bore a strong resemblance to Rambus's own narrow-bus, multiplexed, packetized RDRAM design. As explained elsewhere in this complaint, the wide-bus, non-packetized synchronous DRAM design adopted by JEDEC differed significantly from Rambus's RDRAM design, and hence from the SyncLink design as well. Thus, to the extent Rambus's September 1995 letter could be interpreted to suggest that Rambus might possess relevant intellectual property rights, JEDEC's members would naturally have understood that any such rights related to the SyncLink design, not to the use of certain technologies in the JEDEC standards.

74. In connection with the same incident that gave rise to this September 1995 letter, Crisp and others within Rambus internally debated the extent to which, and manner in which, Rambus should consider making patent-related disclosures to JEDEC or to individual JEDEC members. In this regard, on May 24, 1995, Crisp sent an e-mail to Rambus's CEO, Geoff Tate, as well as other Rambus executives, suggesting a possible bifurcated approach to disclosure. As to any "really key" technologies, Crisp suggested that Rambus should consider making disclosures. But "[i]f it is not a really key issue," Crisp stated, "then … it makes no sense to alert them to a potential problem they can easily work around."

75. In the same e-mail, Crisp outlined a second possible approach to dealing with the disclosure issue:

> "We may want to walk into the next JEDEC meeting and simply provide a list of patent numbers which we have issued and say 'we are not lawyers, we will pass no judgment of infringement or non-infringement, but here are our issued patent numbers, you decide for yourselves what does and does not infringe.'"

Although Rambus in this particular instance did not adopt this approach to disclosure, Crisp's suggestion foreshadowed quite closely the manner in which Rambus would later announce its withdrawal from JEDEC roughly a year later, in June 1996 (*see* Paragraphs 81-88 below).

76. Prior to withdrawing from the organization in June 1996, Rambus did make one patent-related disclosure to JEDEC. In September 1993, Rambus informed JEDEC of the issuance of U.S. Patent No. 5,423,703 (hereinafter, "the '703 patent"). Although the '703 patent claimed priority back to Rambus's '898 application and thus contained the same specification and drawings, the claims of the '703 patent related to a specific clocking technology, unique to RDRAM, that differed significantly from any clocking technology considered by JEDEC. For

this reason, the patent rights conferred upon Rambus by the '703 patent – as reflected in the patent's claims – did not relate to or involve JEDEC's work on SDRAM standards. Furthermore, Rambus's disclosure of this patent did nothing to alert JEDEC's members to Rambus's belief that the specification and related drawings common to the '703 patent and all other patent applications in the '898 family provided a basis upon which it could claim additional patent rights covering technologies incorporated in the SDRAM standards.

77. Other than the foregoing, Rambus made no patent-related disclosures to JEDEC or to the JC-42.3 Subcommittee prior to withdrawing from JEDEC in June 1996. While Rambus was a member of JEDEC, however, some JEDEC members obtained (or viewed) copies of one or more foreign patent applications filed by Rambus, which contained the same specification and drawings as the '898 application and its progeny. In light of the various information (identified in, *inter alia*, Paragraphs 54-55, 60, 64, 68, 70, 73, and 76 above) that Rambus failed to disclose to JEDEC, simply viewing these foreign patent applications would have done nothing to alert JEDEC's members to the fact that Rambus believed the specification and related drawings common to the foreign applications and the '898 family of U.S. patent applications permitted it to claim additional patent rights covering the SDRAM standards.

78. Finally, before, during, and after its tenure as a JEDEC member, in connection with its ongoing efforts to market and license RDRAM, Rambus made limited, private disclosures about its technology to some of the companies participating in JC-42.3. Upon information and belief, these disclosures were made pursuant to agreements prohibiting the company receiving such information from disclosing it to others. In any event, these limited, private disclosures concerning Rambus's proprietary, narrow-bus RDRAM technology were not adequate to satisfy Rambus's disclosure obligations, nor did such disclosures do, or convey, anything to place individual JEDEC members on notice of Rambus's belief that it could claim patent rights over technologies used in the JEDEC SDRAM standards.

Rambus's Violations of the JEDEC Disclosure Duty

79. As discussed above, upon joining JEDEC, Rambus became subject to the same basic disclosure duty applicable to all JEDEC members – the duty to disclose the existence of any patents or pending patent applications it knew or believed "might be involved in" the standard-setting work that JEDEC was undertaking, and to identify the aspect of JEDEC's work to which they related. (*See* Paragraphs 21 and 24 above.)

80. Rambus violated this duty repeatedly, notwithstanding the limited patent-related disclosures discussed above. The fact is that Rambus, while participating as a JEDEC member, possessed a variety of patent applications – and at least one issued patent – that covered, or were designed to cover, technologies involved in the JEDEC standard-setting work, as well as

additional applications that Rambus believed could be amended to cover such technologies without the addition of any new matter. Rambus never disclosed these critical facts to JEDEC.

Rambus's Withdrawal from JEDEC

81. In December 1995, Vincent learned of, and discussed with Anthony Diepenbrock, an in-house Rambus attorney, the Commission's proposed consent order in *In re Dell Computer Corporation*, which involved allegations of anticompetitive unilateral conduct occurring within the context of an industry-wide standard-setting organization. In January 1996, Vincent advised Rambus that it should terminate "further participation in any standards body," including JEDEC.

82. On June 17, 1996, Rambus formally withdrew from JEDEC via a letter addressed to Ken McGhee, an EIA employee who at the time served as Secretary of JEDEC's JC-42 Committee. The letter was originally drafted by Richard Crisp; however, the final version reflected input from Lester Vincent, among others. Other than McGhee, the letter was sent to no one else within JEDEC, including no members of the JC-42.3 Subcommittee.

83. The letter opened by informing Mr. McGhee that Rambus would not be renewing its membership in the various JEDEC committees and subcommittees in which it had participated, including JC-42.3, and that it therefore was returning its membership invoices unpaid. The remainder of the letter stated as follows:

> "Recently at JEDEC meetings the subject of Rambus patents has been raised. Rambus plans to continue to license its proprietary technology on terms that are consistent with the business plan of Rambus, and those terms may not be consistent with the terms set by standards bodies, including JEDEC. A number of major companies are already licensees of Rambus technology. We trust that you will understand that Rambus reserves all rights regarding its intellectual property. Rambus does, however, encourage companies to contact Dave Mooring of Rambus to discuss licensing terms and to sign up as licensees.
>
> To the extent that anyone is interested in the patents of Rambus, I have enclosed a list of Rambus U.S. and foreign patents. Rambus has also applied for a number of additional patents in order to protect Rambus technology."

84. Although it attached a list of 23 Rambus patents, Rambus's June 1996 withdrawal letter said nothing to inform JEDEC how, if at all, the 23 listed patents – and the vague reference to additional, unspecified patent applications – might relate to the work of the JC-42.3 Subcommittee. The unstated message, as Crisp had suggested roughly a year earlier, was:

"[H]ere are our issued patent numbers, you decide for yourselves what does and does not infringe." (*See* Paragraph 75 above.)

85. The list of 23 Rambus patents attached to this letter consisted of 21 U.S. and two foreign (one Taiwanese and one Israeli) patent numbers, with no accompanying explanation.

a. Of the 21 U.S. patents on the list, five fell within the '898 family and the remaining 16 fell outside the '898 family.

b. Of the latter group of 16, several related to discrete designs for generic electronic circuits – that is, they did not relate uniquely to DRAM design or specifically to Rambus's RDRAM architecture. Several other patents included within this group of 16 did relate in some way to DRAM design but did not bear any direct connection to either Rambus's narrow-bus RDRAM architecture or the wide-bus architecture incorporated into the JEDEC SDRAM standards. The remaining few patents from this group of 16 related to specific implementations of Rambus's narrow-bus architecture. There is no indication that any of these 16 patents related to any specific technology or technological feature adopted or considered for adoption in the SDRAM standards.

c. The five U.S. patents that did fall within the '898 family included the '703 patent discussed in Paragraph 76 above, which Rambus had previously disclosed to JEDEC. Of the remaining four, three of the listed patents – like the '703 patent – contained only claims that either (1) were expressly limited to the narrow-bus RDRAM architecture, or (2) dealt with a specific aspect of the Rambus RDRAM architecture unrelated to JEDEC's work. The final patent within this group – U.S. Patent No. 5,473,575 – contained claims that, although potentially broader in scope than the other four, were limited to the low-voltage design used in Rambus's RDRAM architecture, which materially differed from the higher-voltage designs that had been the focus of JEDEC's work.

d. The remaining two Rambus patents on the list of 23 were the two foreign patents. Beyond the fact that one of these was written in Chinese, these foreign patents, had they been reviewed by JEDEC's members, would not have sufficed to place them on notice of Rambus's patent rights, or potential patent rights, for reasons discussed above.

86. More important than what the June 1996 withdrawal letter said is what it failed to say. Among other things, the letter made no mention of the fact that Rambus possessed pending patent applications covering, or that could be amended to cover, specific technologies included, or proposed for inclusion, in the JEDEC SDRAM standards. Nor did the letter say anything to

alert JEDEC to Rambus's belief that it could claim rights to certain technological features not only when used in the context of its proprietary, narrow-bus, RDRAM designs, but also when used in the traditional wide-bus architecture that was the focus of JEDEC's SDRAM standard-setting activities.

87. But this was not all the June 1996 letter failed to disclose. As of June 1996, when Rambus submitted its formal withdrawal letter to JEDEC, the company actually possessed 24 issued patents, not 23. That is, one – but only one – of Rambus's issued patents was omitted from the list attached to the June 1996 withdrawal letter. The omitted patent was Rambus's '327 patent, which issued in April 1996, two months before Rambus's withdrawal from JEDEC. As discussed in Paragraph 68 above, the '327 patent contained claims purporting to cover use of dual-edge clock technology in any synchronous DRAM architecture. As such, it was the only patent actually obtained by Rambus while a member of JEDEC that arguably covered use of a specific technology included, or considered for inclusion, in JEDEC's wide-bus SDRAM standards.

88. Even after withdrawing from JEDEC, Crisp and others within Rambus continued to closely monitor JEDEC's ongoing work on SDRAM standards, including work involving specific technologies on which Rambus sought to perfect patent rights.

Industry Adoption of the JEDEC Standards

89. In the years following the issuance of JEDEC's first SDRAM standard in November 1993, DRAM manufacturers and their customers began designing, testing, and ultimately manufacturing memory and memory-related products incorporating, or complying with, JEDEC's standardized SDRAM designs. By 1995, JEDEC-compliant SDRAM had begun to replace older-generation, asynchronous DRAM architectures. Thereafter, the shift to the more modern SDRAM technology progressed rapidly. By 1998, total worldwide sales of JEDEC-compliant SDRAM, on a revenue basis, exceeded sales of asynchronous memory. And by 1999, JEDEC-compliant SDRAM had largely replaced asynchronous DRAM in virtually all relevant uses. Toward the end of this period – roughly 1999 to 2000 – some DRAM manufacturers and their customers also began using RDRAM, but only in very limited end uses, accounting for a relatively small portion (*i.e.*, in the range of 5%) of overall DRAM production.

90. Leading up to and following the issuance of JEDEC's second-generation SDRAM standard – or DDR SDRAM – in August 1999, DRAM manufacturers and their customers began designing, testing, and (to a limited extent) producing memory and memory-related products incorporating, or complying with, the DDR SDRAM standard. By 2000, DDR SDRAM was beginning to be manufactured in increasing volumes. This trend continued during 2001, and a number of DRAM manufacturers and their customers began to replace first-generation

SDRAM and RDRAM with DDR SDRAM for certain high-end uses. Current projections indicate that total sales of DDR SDRAM, on a revenue basis, may account for as large as 40% of all DRAM produced worldwide in 2002, and by 2004 this figure is expected to exceed 50%.

Success of Rambus's Scheme

91. Throughout the late 1990s, as the DRAM industry became increasingly locked in to use of JEDEC-compliant SDRAM, and subsequently DDR SDRAM, Rambus continued the process of perfecting patent rights on certain technologies incorporated within the JEDEC SDRAM standards. By the late 1990s, Rambus had succeeded in obtaining numerous patents, not expressly limited to a narrow-bus RDRAM architecture, that purported to cover, among other technologies encompassed by the JEDEC standards, programmable CAS latency, programmable burst length, on-chip DLL, and dual-edge clock.

92. In late 1999, Rambus began contacting all major DRAM and chipset manufacturers worldwide asserting that, by virtue of their manufacture, sale, or use of JEDEC-compliant SDRAM, they were infringing upon Rambus's patent rights, and inviting them to contact Rambus for the purpose of promptly resolving the issue.

93. Thereafter, Rambus entered into license agreements with seven major DRAM manufacturers: Matsushita Electric Industrial Co., Ltd.; Elpida Memory, Inc.; Samsung Electronics Co.; NEC Corporation; Toshiba America Inc.; Oki Electric Industry Co.; and Mitsubishi Electronics America Inc. Pursuant to these licenses, Rambus allowed each company to use those aspects of its technology necessary for the design and manufacture of JEDEC-compliant SDRAM. In exchange, each company agreed to pay Rambus ongoing royalties reflecting 0.75% of revenues associated with the manufacture and sale of SDRAMs and 3.5% of revenues associated with the manufacture and sale of DDR SDRAMs. By comparison, Rambus typically licenses all the information needed to develop Rambus-compatible RDRAM memory at royalty rates ranging up to a maximum of approximately 2.5% of revenues.

94. After disclosing its patents, Rambus stated publicly that it would demand even higher royalties from any DRAM manufacturer that refused to license the Rambus patents and instead chose to litigate. Rambus also publicly threatened that it might simply refuse to license its patents to any DRAM manufacturer that was unsuccessful in litigation.

95. In January 2000, Rambus filed the first in a series of patent infringement suits. That suit, which was filed in federal district court in Delaware and named only one defendant – Hitachi – was subsequently settled, conditioned upon Hitachi's agreement to submit to Rambus's license terms.

96. With the signing of the Hitachi license, combined with the seven additional licenses discussed above, Rambus had succeeded in obtaining licenses covering roughly 50% of total worldwide production of synchronous DRAM technology. At current market prices for SDRAM, such licenses entitle Rambus to royalties in the range of $50-100 million per year, a number that could increase significantly in the event Rambus were to prevail in the ongoing litigation and secure licenses from the remaining manufacturers of SDRAMs. Indeed, under such circumstances, Rambus's SDRAM-related patent rights could allow Rambus to extract royalty payments well in excess of a billion dollars from the DRAM industry over the life of the patents.

97. In August 2000, Rambus filed suit against another DRAM manufacturer – Infineon – in federal district court in Virginia, accusing Infineon of patent infringement. Infineon later asserted various affirmative defenses and counterclaims. In April 2001, the case proceeded to trial, resulting in a jury finding of fraud against Rambus relating to its involvement in the standard-setting activities of JC-42.3 and a legal ruling that Rambus's patents were not infringed by Infineon's use of the SDRAM standards. These and other legal issues are currently pending on appeal before the U.S. Court of Appeals for the Federal Circuit, which heard oral argument June 3, 2002. (Infineon's antitrust claim against Rambus was dismissed due to a technical failure of proof concerning the relevant geographic market. This ruling has not been appealed.)

98. Also in August 2000, Rambus itself was sued, in federal district court in California, by another DRAM manufacturer – Hynix – seeking a declaratory judgment that its manufacture and sale of JEDEC-compliant SDRAM did not infringe Rambus's patents. In addition to seeking declaratory relief, Hynix accuses Rambus of, among other things, antitrust violations, unfair competition, and breach of contract. Meanwhile, Rambus counterclaimed, alleging patent infringement, and the suit was subsequently stayed pending a ruling by the Federal Circuit in the *Infineon* litigation.

99. In a second suit filed against Rambus in August 2000, in federal district court in Delaware, another major DRAM manufacturer – Micron – seeks a declaratory judgment that its manufacture and sale of JEDEC-compliant SDRAM does not infringe Rambus's patents. In addition to seeking declaratory relief, Micron accuses Rambus of monopolization, attempted monopolization, fraud, and inequitable conduct. As in the *Hynix* suit, Rambus has asserted counterclaims against Micron, accusing it of patent infringement, and the suit has been stayed, at least for purposes other than discovery, pending resolution of the *Infineon* appeal.

100. In the *Infineon*, *Hynix*, and *Micron* lawsuits combined, Rambus has asserted that a dozen or more of its patents have been infringed through the production and sale of JEDEC-compliant SDRAM by these three companies. Each of the patents upon which Rambus has sued stems from, and claims priority back to, Rambus's '898 application.

101. Upon information and belief, Rambus also possesses additional patents and patent applications, some claiming priority back to the '898 application, that it has not yet sought, but could in the future seek, to enforce against memory manufacturers producing JEDEC-compliant SDRAM, absent issuance of the relief requested below.

102. In addition to the foregoing, Rambus is involved in other litigation in various foreign countries relating to foreign patents that cover, or purport to cover, many of the same DRAM-related technologies that are at issue in the U.S. litigation.

103. Notably, while Rambus has licenses covering roughly 50% of the synchronous DRAM industry, Rambus asserts in litigation that all or virtually all synchronous DRAM produced worldwide incorporates Rambus technology and that those synchronous DRAM manufacturers that are not paying royalties to Rambus are liable in damages. In addition to facing the threat of potential damages, those companies that have chosen to litigate against Rambus have been forced to incur substantial litigation costs, reaching into the millions, if not tens of millions, of dollars. Unless they prevail against Rambus in litigation, such companies also face the prospect of being denied licenses to Rambus's patents, or otherwise being required to pay royalties significantly in excess of the amounts paid by the memory manufacturers that acquiesced to Rambus's licensing demands without resort to litigation.

104. Rambus also has licensed companies, such as Intel, that do not produce memory chips but do produce related computer components – in Intel's case, chipsets – that are designed to be compatible with synchronous DRAMs.

Inability of DRAM Industry to Work Around Rambus's Patents

105. Given the extensive degree to which the DRAM industry has become locked in to the JEDEC SDRAM standards, it is not economically feasible for the industry to attempt to alter or work around the JEDEC standards in order to avoid payment of royalties to Rambus. Any such effort would face innumerable practical and economic impediments, including but not limited to the out-of-pocket costs associated with redesigning, validating, and qualifying SDRAM products to conform with a revised set of standards. On top of this, such manufacturers could be forced to absorb potentially massive revenue losses if, as a result of modifying the JEDEC standards, their introduction of new products were delayed.

106. Agreeing upon revised SDRAM standards could in itself be a very costly and time-consuming process. Indeed, it is unclear whether the industry would be able to reach any such consensus, given complications inherent in the current market environment, including the fact that some DRAM manufacturers have acquiesced to Rambus's licensing demands while others have not.

107. Added to these complications is the fact that purchasers and other users of JEDEC-compliant SDRAM technology – including manufacturers of computers, chipsets, graphics cards, and motherboards – have themselves become locked in to the JEDEC standards. For this and other reasons, even if the DRAM industry were otherwise able to undertake the complicated and costly task of revising the JEDEC standards to work around Rambus's patent claims, it is unclear whether downstream purchasers of synchronous DRAM would welcome or accept such an action, given the costs that they would be forced to incur in order to conform their own product designs and manufacturing processes to a revised set of standards. Nor is it clear whether downstream purchasers and other users of SDRAM technology would tolerate the delay in the introduction of new products that likely would result from the process of changing the standard.

108. Any effort to revise the JEDEC standards on a going-forward basis could also interfere with the ability of DRAM designers, manufacturers, and users to maintain the backwards compatibility among successive generations of synchronous DRAM that JEDEC has sought to preserve.

109. For these and other reasons, the DRAM industry has had little or no practical ability to work around Rambus's patent claims, and it is not at all clear the industry could do so in the future.

Relevant Product Markets

110. Synchronous DRAM is produced throughout the world by various memory manufacturers located or doing business in the U.S. and various foreign countries. Synchronous DRAMs, and products incorporating synchronous DRAMs, are imported and exported throughout the world in large volumes.

111. Commercial DRAM chip manufacturers wishing to design and produce synchronous DRAM chips, wherever they may be located throughout the world, are practically limited to using one of two alternative architectures: the JEDEC-compliant SDRAM architecture or Rambus's own proprietary RDRAM architecture, itself a synchronous DRAM technology. No other synchronous DRAM architectures have been developed and made available for wide-spread commercial use.

112. The RDRAM and JEDEC-compliant SDRAM architectures, in turn, each consist of a variety of subsidiary technologies – or technological features – that are necessary in order successfully to design and manufacture a synchronous DRAM chip. These subsidiary technologies may be regarded as essential technology inputs into the design and manufacture of synchronous DRAMs.

113. As in other aspects of engineering, electrical engineers involved in the design of synchronous DRAM chips select from among alternative technological features, concepts, or approaches in

order to address or solve issues, or problems, that arise in the course of developing such chips. The alternative technologies available to address a given technical issue arising in the course of synchronous DRAM design together may comprise a separate, well-defined product market. At least four such markets are relevant for purposes of the instant complaint, including the following:

a. The market for technologies used to specify the length of time – or "latency" period – between the memory's receipt of a read request and its release of data corresponding with the request (hereinafter, the "latency technology market"). This market includes programmable CAS latency and any alternative technologies that may be economically viable substitutes for the use of programmable CAS latency in synchronous DRAM design.

b. The market for technologies used to specify the number of times information (data) is transmitted between the CPU and memory – *i.e.*, the "burst length" – associated with a single request or instruction (hereinafter, the "burst length technology market"). This market includes programmable burst length and any alternative technologies that may be economically viable substitutes for the use of programmable burst length in synchronous DRAM design.

c. The market for technologies used to synchronize the internal clock that governs operations within a memory chip and the system clock that regulates the timing of other system functions (hereinafter, the "clock synchronization technology market"). This market includes on-chip DLL technology and any alternative technologies that may be economically viable substitutes for the use of an on-chip DLL in synchronous DRAM design.

d. The market for technologies used to accelerate the rate at which data are transmitted between the CPU and memory (hereinafter, the "data acceleration technology market"). This market includes dual-edge clock technology and any alternative technologies that may be economically viable substitutes for the use of a dual-edge clock in synchronous DRAM design.

114. Technologies used in the design of synchronous DRAM chips, to solve separate but related design issues, may be viewed as economic complements. The complementary nature of such design technologies is evidenced by, among other things, the fact that they sometimes are licensed together in a package, as is the case with respect to the patented Rambus technologies encompassed by each of the aforementioned product markets. Where such close relationships exist among a group of technologies, all of which are necessary inputs into the design or manufacture of a common downstream product, one may appropriately define a product

market encompassing the group of complementary technologies and their close substitutes. Thus, in addition, or in the alternative, to the four product markets identified above, there is a fifth well-defined product market that is relevant for purposes of this complaint – namely, a market comprising, collectively, all technologies falling within any one of these narrower markets (hereinafter, the "synchronous DRAM technology market").

Geographic Scope of Relevant Product Markets

115. Technologies encompassed within each of the foregoing product markets are used on a worldwide basis. Technologies originating outside the United States frequently are considered for and used in JEDEC standards, and indeed have been used in both the first- and second-generation SDRAM standards promulgated by JEDEC. The technologies selected for inclusion in these JEDEC standards, in turn, have been incorporated and used by synchronous DRAM manufacturers throughout the world.

116. Both proprietary and non-proprietary technologies have been used in synchronous DRAM design. To the extent such technologies are non-proprietary, they are free to be used, on a non-royalty-incurring basis, by any synchronous DRAM manufacturer or downstream user worldwide. On the other hand, to the extent such technologies are proprietary, inasmuch as they are subject to patents or potential patent claims in one or more jurisdictions, the use of such technologies by synchronous DRAM manufacturers or downstream users may depend upon the user's agreement to specific license terms negotiated with the patent holder. In the event that patent rights are similar in most relevant jurisdictions, however, there is no apparent legal or economic impediment that would preclude licenses from being made available on a multi-national or worldwide basis. Indeed, Rambus, which holds synchronous DRAM-related patents issued in the United States and numerous foreign countries, commonly grants licenses to companies in the U.S. and abroad encompassing rights to use Rambus's patented technologies worldwide.

117. For these and other reasons, each of the technology-related product markets identified above is worldwide in scope.

118. Alternatively, or in addition, the geographic scope of such product markets might appropriately be defined as the United States if, for example, Rambus's U.S. patent rights differed significantly from rights recognized in various foreign jurisdictions, or if Rambus otherwise had the ability to vary royalty rates from one jurisdiction to another.

Anticompetitive Effects of Rambus's Conduct

119. The foregoing conduct by Rambus, during and after its involvement in JEDEC's JC-42.3 Subcommittee, has materially caused or threatened to cause substantial harm to competition and will, in the future, materially cause or threaten to cause further substantial injury to competition and consumers, absent the issuance of appropriate relief in the manner set forth below.

120. The threatened or actual anticompetitive effects of Rambus's conduct include but are not limited to the following:

a. increased royalties (or other payments) associated with the manufacture, sale, or use of synchronous DRAM technology;

b. increases in the price, and/or reductions in the use or output, of synchronous DRAM chips, as well as products incorporating or using synchronous DRAMs or related technology;

c. decreased incentives, on the part of memory manufacturers, to produce memory using synchronous DRAM technology;

d. decreased incentives, on the part of DRAM manufacturers and others, to participate in JEDEC or other industry standard-setting organizations or activities; and

e. both within and outside the DRAM industry, decreased reliance, or willingness to rely, on standards established by industry standard-setting collaborations.

Rambus's Knowing Destruction of Documents

121. Rambus has engaged in a systematic effort – blessed if not orchestrated by its most senior executives – to destroy documents and other information. Upon information and belief, among other pertinent files destroyed as a result of this campaign were notes and other documentation relating to, among other things, Rambus's involvement in the JC-42.3 Subcommittee. Upon information and belief, this document-destruction campaign was undertaken, wholly or in substantial part, with the purpose of avoiding or minimizing the adverse legal repercussions of the anticompetitive conduct described in the instant complaint. Partly as a consequence of these document-destruction activities, in combination with other bad-faith litigation conduct, Rambus was required by the federal district court presiding over the *Infineon* litigation to pay a sanction exceeding $7 million.

First Violation Alleged

122. As described in Paragraphs 1-121 above, which are incorporated herein by reference, Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, undertaken over the course of the past decade, and continuing even today, whereby it has obtained monopoly power in the synchronous DRAM technology market and narrower markets encompassed therein – namely, the latency, burst length, clock synchronization, and data acceleration markets discussed above – which acts and practices constitute unfair methods of competition in violation of Section 5 of the FTC Act.

Second Violation Alleged

123. As described in Paragraphs 1-121 above, which are incorporated herein by reference, Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, undertaken over the course of the past decade, and continuing even today, with a specific intent to monopolize the synchronous DRAM technology market and narrower markets encompassed therein, resulting, at a minimum, in a dangerous probability of monopolization in each of the aforementioned markets, which acts and practices constitute unfair methods of competition in violation of Section 5 of the FTC Act.

Third Violation Alleged

124. As described in Paragraphs 1-121 above, which are incorporated herein by reference, Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, undertaken over the course of the past decade, and continuing even today, whereby it has unreasonably restrained trade in the synchronous DRAM technology market and narrower markets encompassed therein, which acts and practices constitute unfair methods of competition in violation of Section 5 of the FTC Act.

Notice

Notice is hereby given to the Respondent that the eighteenth day of September, 2002, at 10:00 a.m., or such later date as determined by an Administrative Law Judge of the Federal Trade Commission, is hereby fixed as the time and Federal Trade Commission offices, 600 Pennsylvania Avenue, N.W., Room 532, Washington, D.C. 20580, as the place when and where a hearing will be had before an Administrative Law Judge of the Federal Trade Commission, on the charges set forth in this complaint, at which time and place you will have the right under the FTC Act to appear and show cause why an order should not be entered requiring you to cease and desist from the violations of law charged in the complaint.

You are notified that the opportunity is afforded to you to file with the Commission an answer to this complaint on or before the twentieth (20th) day after service of it upon you. An answer in which the allegations of the complaint are contested shall contain a concise statement of the facts constituting each ground of defense; and specific admission, denial, or explanation of each fact alleged in the complaint or, if you are without knowledge thereof, a statement to that effect. Allegations of the complaint not thus answered shall be deemed to have been admitted.

If you elect not to contest the allegations of fact set forth in the complaint, the answer shall consist of a statement that you admit all of the material facts to be true. Such an answer shall constitute a waiver of hearings as to the facts alleged in the complaint and, together with the complaint, will provide a record basis on which the Administrative Law Judge shall file an initial decision containing appropriate findings and conclusions and an appropriate order disposing of the proceeding. In such answer, you may, however, reserve the right to submit proposed findings and conclusions under § 3.46 of the Commission's Rules of Practice for Adjudicative Proceedings and the right to appeal the initial decision to the Commission under § 3.52 of said Rules.

Failure to answer within the time above provided shall be deemed to constitute a waiver of your right to appear and contest the allegations of the complaint and shall authorize the Administrative Law Judge, without further notice to you, to find the facts to be as alleged in the complaint and to enter an initial decision containing such findings, appropriate conclusions, and order.

The ALJ will schedule an initial prehearing scheduling conference to be held not later than 14 days after the last answer is filed by any party named as a respondent in the complaint. Unless otherwise directed by the ALJ, the scheduling conference and further proceedings will take place at the Federal Trade Commission, 600 Pennsylvania Avenue, N.W., Room 532, Washington, D.C. 20580. Rule 3.21(a) requires a meeting of the parties' counsel as early as practicable before the prehearing scheduling conference, and Rule 3.31(b) obligates counsel for each party, within 5 days of receiving a respondent's answer, to make certain initial disclosures without awaiting a formal discovery request.

Notice of Contemplated Relief

Should the Commission conclude from the record developed in any adjudicative proceedings in this matter that Respondent's conduct violated Section 5 of the Federal Trade Commission Act as alleged in the complaint, the Commission may order such relief as is supported by the record and is necessary and appropriate, including but not limited to:

1. Requiring Respondent to cease and desist all efforts it has undertaken by any means, including without limitation the threat, prosecution, or defense of any suits or other actions, whether legal, equitable, or administrative, as well as any arbitration, mediation, or any other form of private dispute resolution, through or in which Respondent has asserted that any person or entity, by manufacturing, selling, or otherwise using JEDEC-compliant SDRAM and DDR SDRAM technology (including future variations of JEDEC-compliant SDRAM and DDR SDRAM technology), infringes any of Respondent's current or future United States patents that claim priority back to U.S. Patent Application Number 07/510,898 filed on April 18, 1990 or any other U.S. Patent Application filed before June 17, 1996.

2. Requiring Respondent not to undertake any new efforts by any means, including without limitation the threat, prosecution, or defense of any suits or other actions, whether legal, equitable, or administrative, as well as any arbitration, mediation, or any other form of private dispute resolution, through or in which Respondent has asserted that any person or entity, by manufacturing, selling, or otherwise using JEDEC-compliant SDRAM and DDR SDRAM technology (including future variations of JEDEC-compliant SDRAM and DDR SDRAM technology), infringes any of Respondent's current or future United States patents that claim priority back to U.S. Patent Application Number 07/510,898 filed on April 18, 1990 or any other U.S. Patent Application filed before June 17, 1996.

3. Requiring Respondent to cease and desist all efforts it has undertaken by any means, including without limitation the threat, prosecution, or defense of any suits or other actions, whether legal, equitable, or administrative, as well as any arbitration, mediation, or any other form of private dispute resolution, through or in which Respondent has asserted that any person or entity, by manufacturing, selling, or otherwise using JEDEC-compliant SDRAM and DDR SDRAM technology (including future variations of JEDEC-compliant SDRAM and DDR SDRAM technology), for import or export to or from the United States, infringes any of Respondent's foreign patents, current or future, that claim priority back to U.S. Patent Application Number 07/510,898 filed on April 18, 1990 or any other Patent Application filed before June 17, 1996.

4. Requiring Respondent not to undertake any new efforts by any means, including without limitation the threat, prosecution, or defense of any suits or other actions, whether legal,

equitable, or administrative, as well as any arbitration, mediation, or any other form of private dispute resolution, through or in which Respondent has asserted that any person or entity, by manufacturing, selling, or using JEDEC-compliant SDRAM and DDR SDRAM technology (including future variations of JEDEC-compliant SDRAM and DDR SDRAM technology), for import or export to or from the United States, infringes any of Respondent's foreign patents, current or future, that claim priority back to U.S. Patent Application Number 07/510,898 filed on April 18, 1990 or any other Patent Application filed before June 17, 1996.

5. Requiring Respondent to employ, at Respondent's cost, a Commission-approved compliance officer who will be the sole representative of Respondent for the purpose of communicating Respondent's patent rights related to any standard under consideration by any standard-setting organization of which Respondent is a member.

6. Such other or additional relief as is necessary to correct or remedy the violations alleged in the complaint.

WHEREFORE, THE PREMISES CONSIDERED, the Federal Trade Commission on this eighteenth day of June, 2002, issues its complaint against said Respondent.

By the Commission.

Donald S. Clark
Secretary